

COMPAL CONFIDENTIAL

MODEL NAME : ZAM70  
PCB NO : DAA0007U000  
BOM P/N : 4319R031L01 (SMT MB AA901 ZAM70 U W/DOCK I5 1.9G R1)  
4319R031L02 (SMT MB AA901 ZAM70 U W/DOCK I3 1.9G R1)  
GPIO MAP: 3.6C

1 chip XDP debug component list(CXDP@)			
item	Qty	Part reference	Part description
1	2	CC17,CC21	SE00000G880 (S CER CAP 0.1U 25V K X5R 0402)
2	4	RC98,RC99,RC109,RC112	SD028000080 (S RES 1/16W 0 +-5% 0402)
3	4	RC102,RC106,RC113,RC120	SD028100180 (S RES 1/16W 1K +-5% 0402)
4	1	UC7	SA00005X900 (S IC 74CBTLV3126BQ DHVQFN 14P BUS SWITCH)
5	1	JXDP1	SP02000L900 (S W-CONN SAMTEC BSH-030-01-L-D-A-TR 60P)

Huston 14" UMA

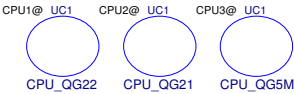
Broadwell U

2014-03-07

REV : 0.3 (X01)

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@ : Nopop Component  
EMC@ : EMI, ESD and RF Component  
@EMC@ : EMI, ESD and RF Nopop Component  
CXDP@ : XDP Component  
VPRO@ : Support VPRO  
CONN@ : Connector Component



MB PCB	
Part Number	Description
DAA00070000	PCB 130 LA-A901P REV0 MB/UMA DOCK 1

Layout Dell logo

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REV: X01  
PWB: DKNFC  
DATE: 1410-06

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Cover Sheet

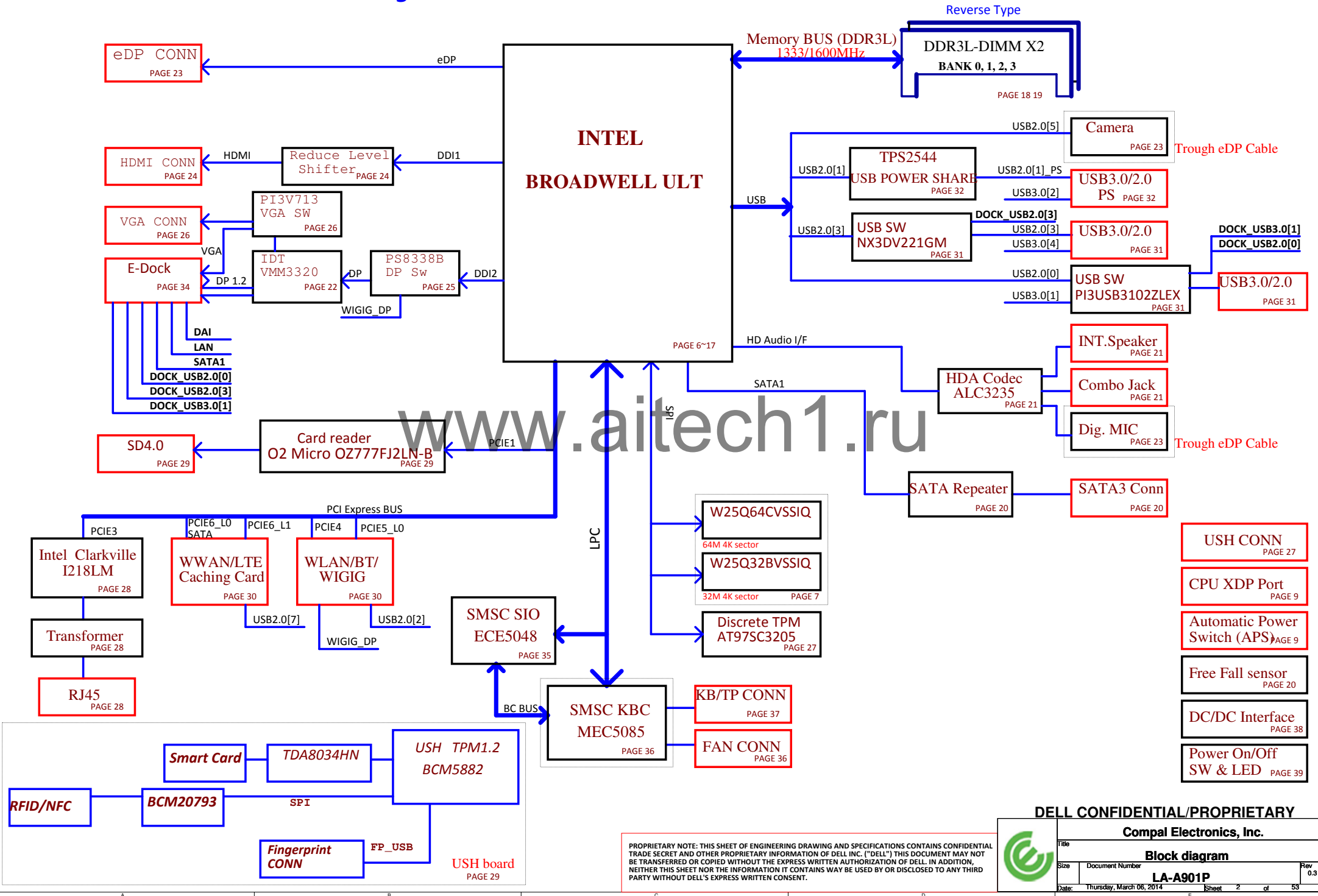
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# Houston 14 UMA Dock Block Diagram



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## POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

## PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE +1.5V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and  
PM Table

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN
PCIE 5			WIGIG
PCIE 6	L3	SATA 0	JDOCK1 (DOCK)
	L2	SATA 1	JSATA1 (HDD)
	L1	SATA 2	SSD Cache (PCIE)
	L0	SATA 3	SSD Cache (SATA/PCIE)/HCA

USB PORT #	DESTINATION
0	JUSB1
1	JUSB3
2	WLAN + BT
3	JUSB2
4	Touch Screen
5	CAMERA
6	USH
7	WWAN

USH	0	BIO
	1	NA

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Port assignment

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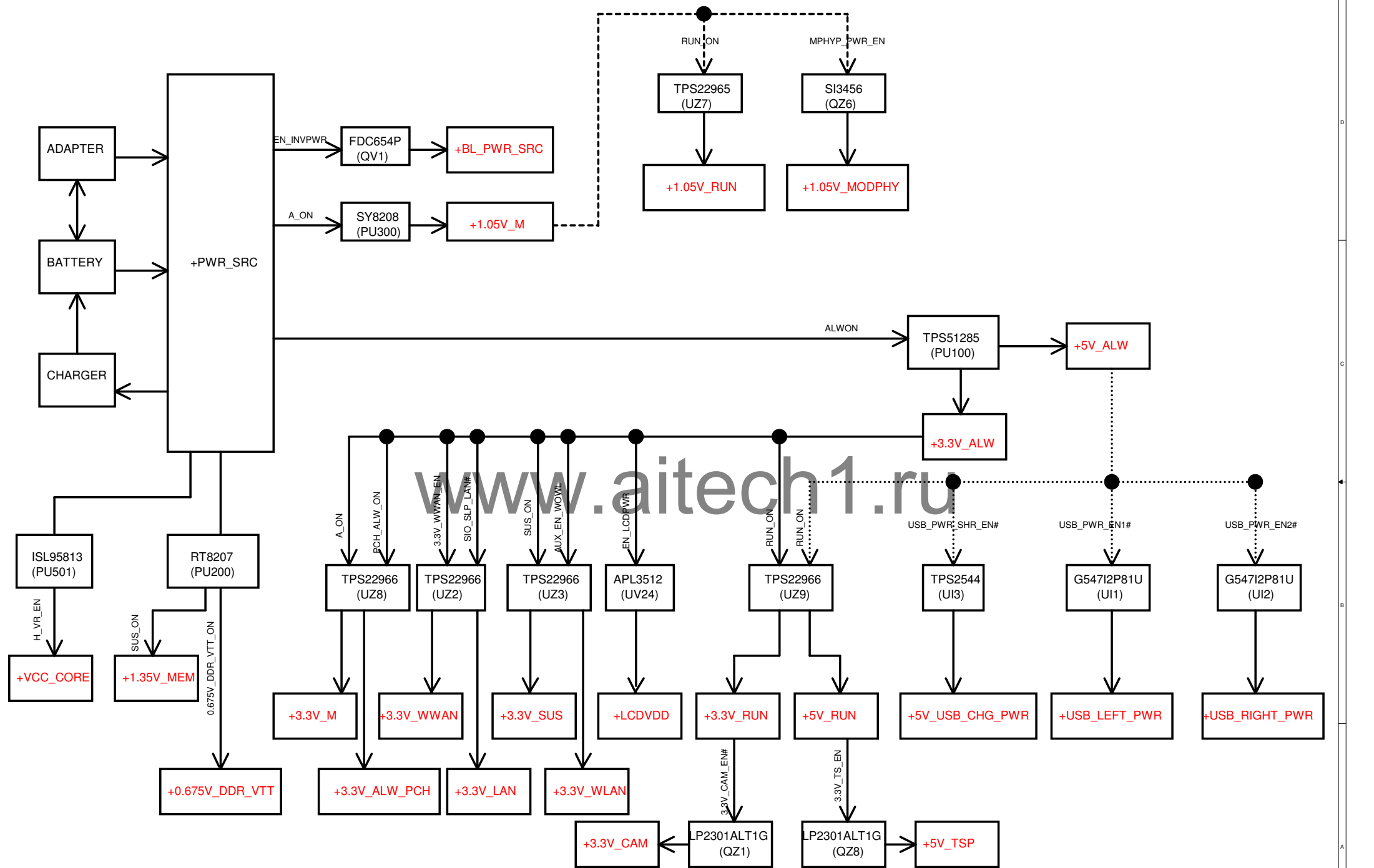
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**Power rails**

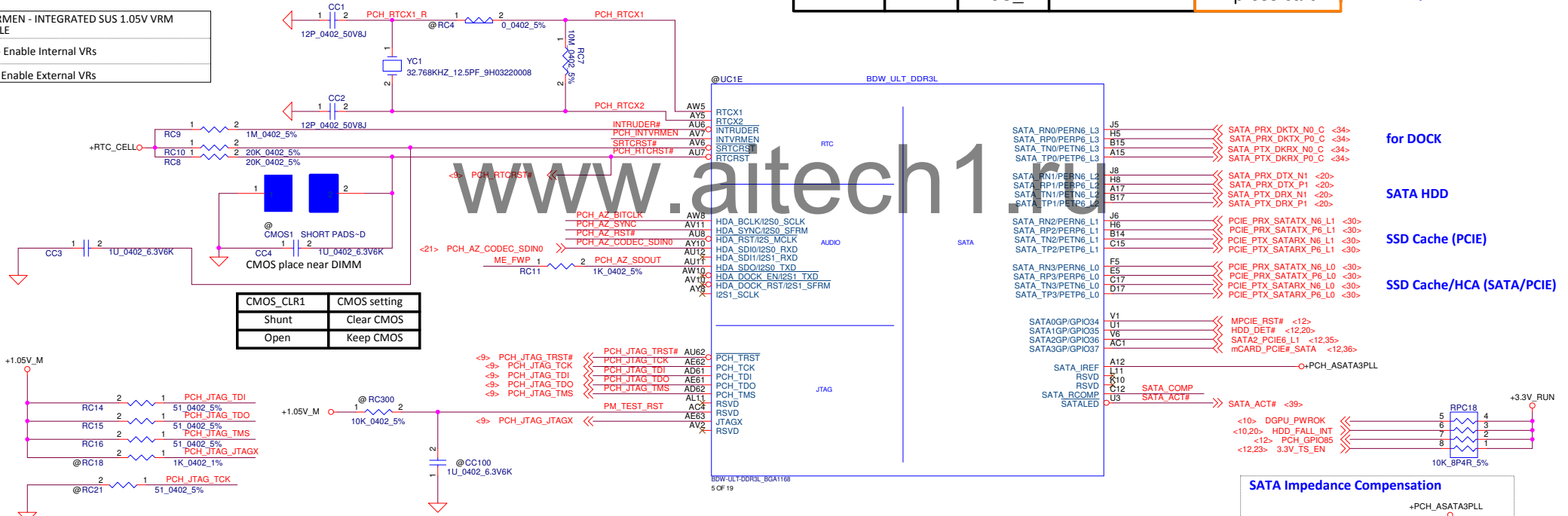
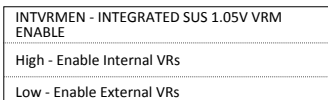
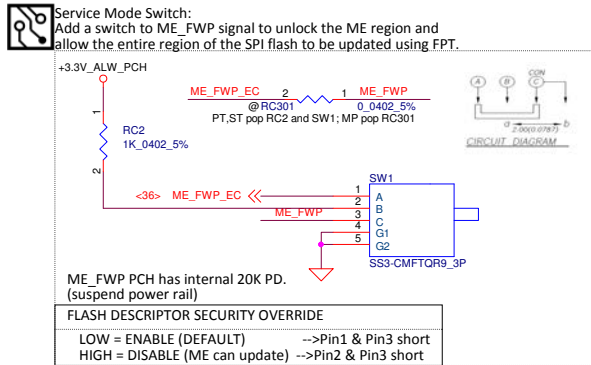
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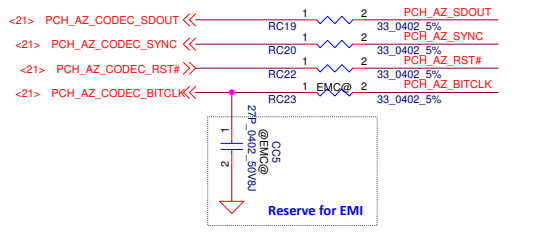
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## UMA SATA port



## HDA for Codec



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SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0
E-Dock	HDD	H12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H12 Entry	NA	NA
E-Dock	HDD	H14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG
E-Dock	HDD	H14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H14D_En	NA	M2 3030 WIGIG
NA	HDD	H14U_En	NA	NA
E-Dock	HDD	H15 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG
E-Dock	HDD	H15 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H15D_En	NA	M2 3030 WIGIG
NA	HDD	H15U_En	NA	Express card

**contact to WWAN**

SATA2/PCIE6\_L1 contact to WWAN  
SATA3/PCIE6 L0 contact to WLAN

**contact to WWAN**

## contact to WLAN

SATA2/PCIE6\_L1 contact to WWAN  
SATA3/PCIE6 L0 contact to WLAN

**contact to WWAN**

### contact to WLAN

1. **Identify the main components of the system.**

contact to Express card

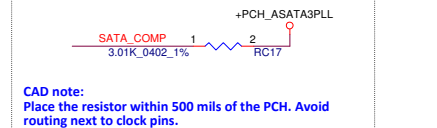
for DOCK

## SATA HDD

### SSD Cache (PCIE)

SSD Cache/HCA (SATA/PCIE)

## SATA Impedance Compensation



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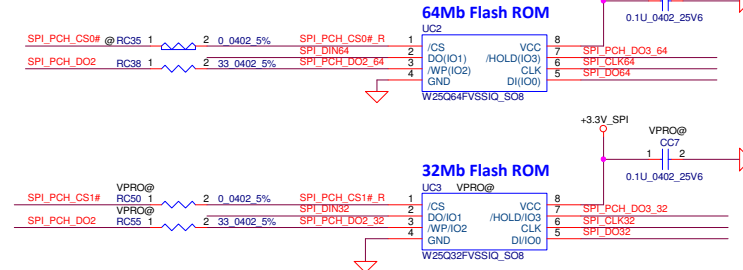
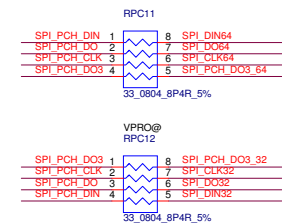
**CPU (1/12)**

**LA-A901P**

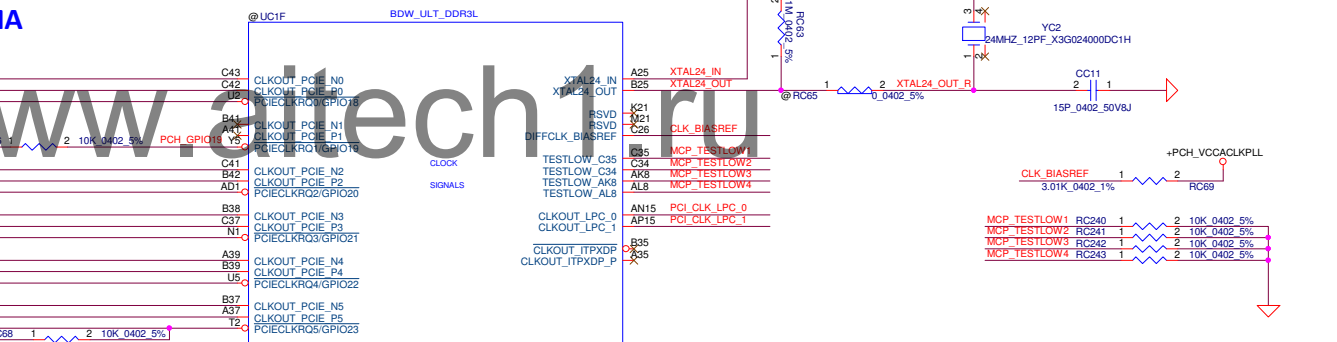
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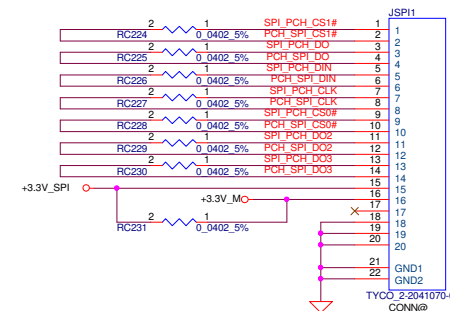
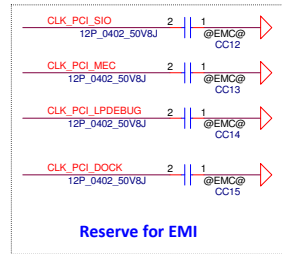
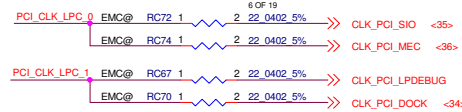
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HCA/PCIe cache (NGFF2)--->



PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	NA



support SPI TPM	
LPC_0	LPC_1
SIO MEC	DOCK DEBUG

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CPU (2/12)

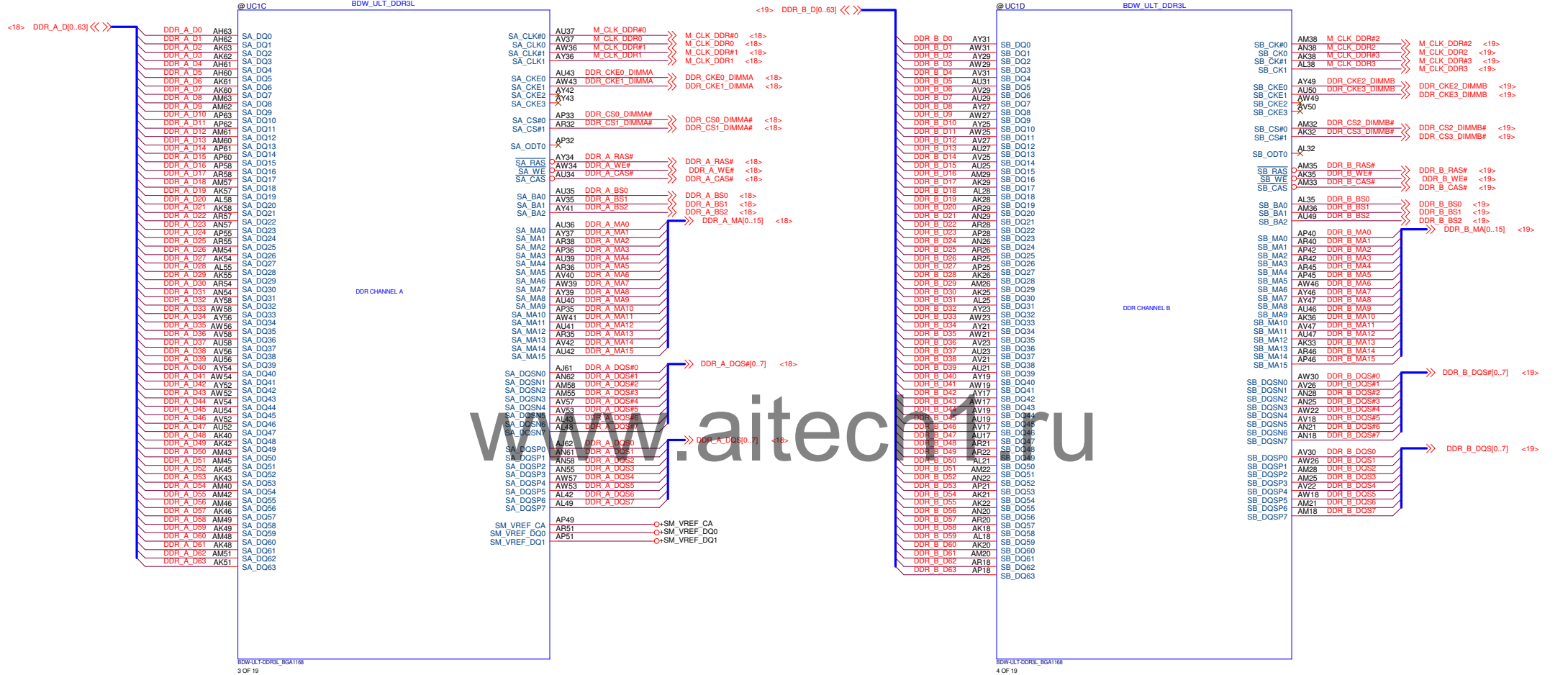
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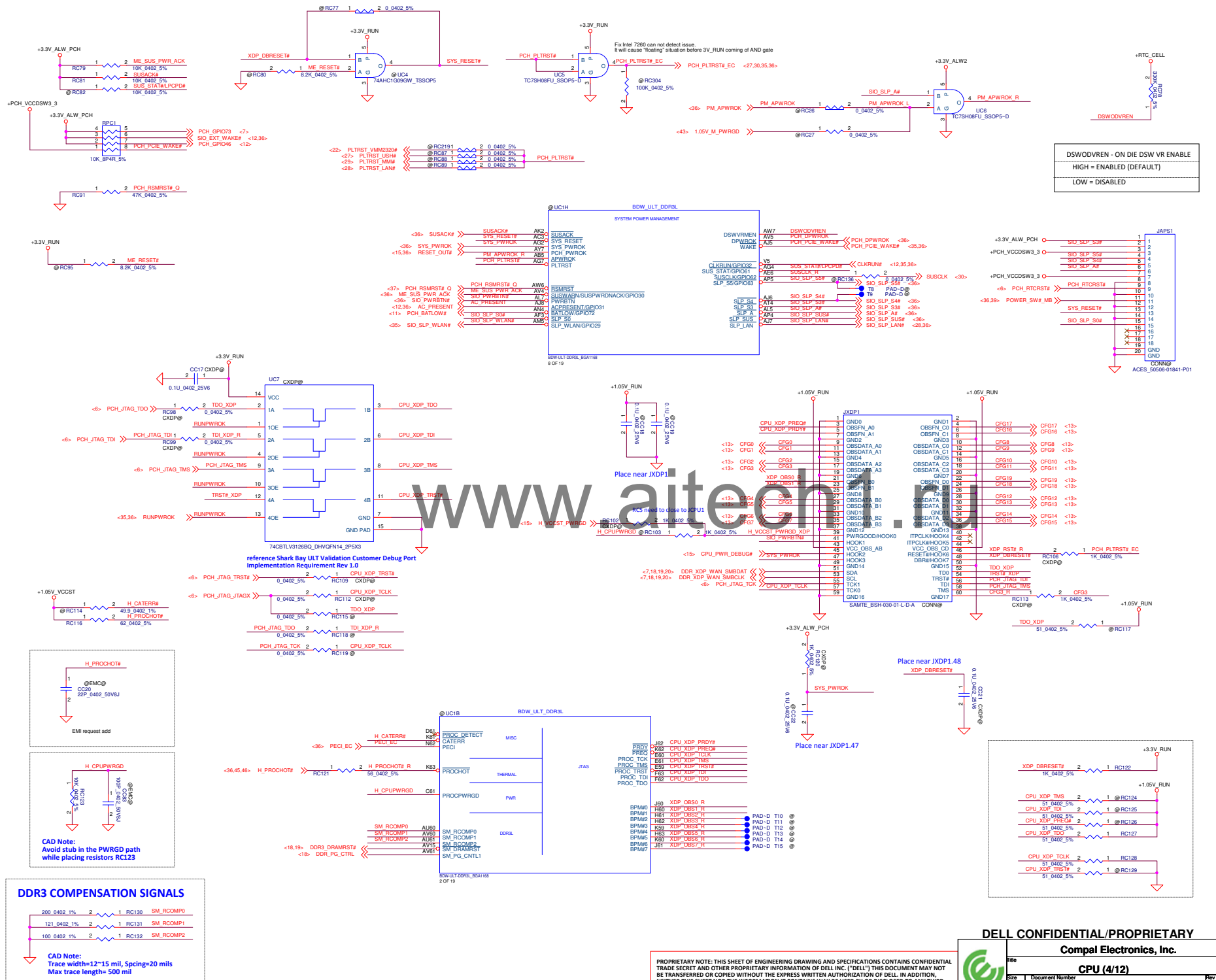
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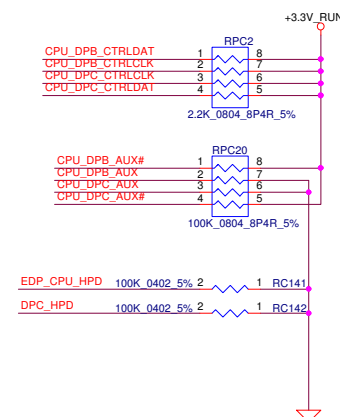
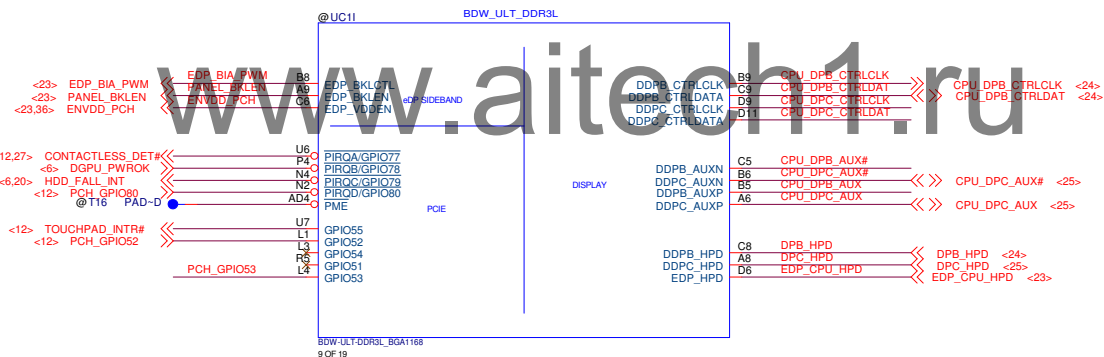
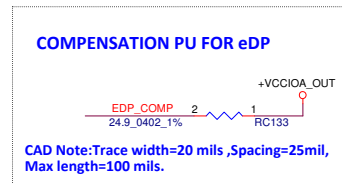




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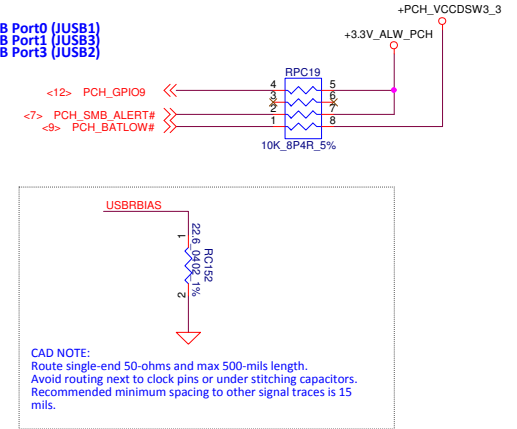


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
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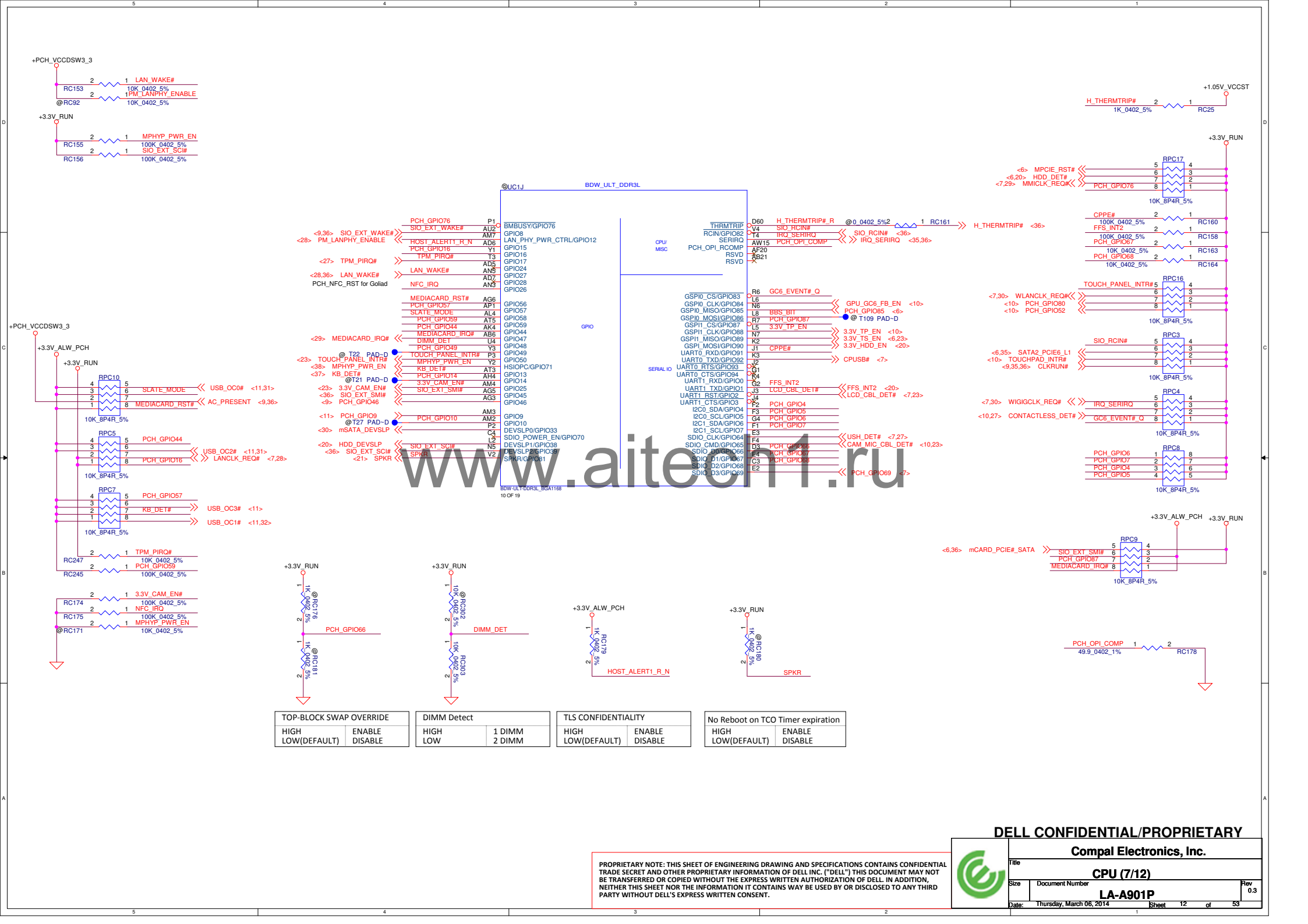
Pinout diagram for the USB connector of the AITECHN1 board. The diagram shows the connection of various pins to the USB connector. The pins are labeled as follows:

- F15
- G15
- B31
- A31
- PERN2/USB3RN4
- PERP2/USB3RP4
- PETN2/USB3TN4
- PETP2/USB3TP4
- USB3RBIAS
- AN10
- R5VD
- R5VD
- OC0GP0Q0
- OC1GP0Q1
- AL3
- AT1
- AP2
- USB\_OC0#
- USB\_G0#

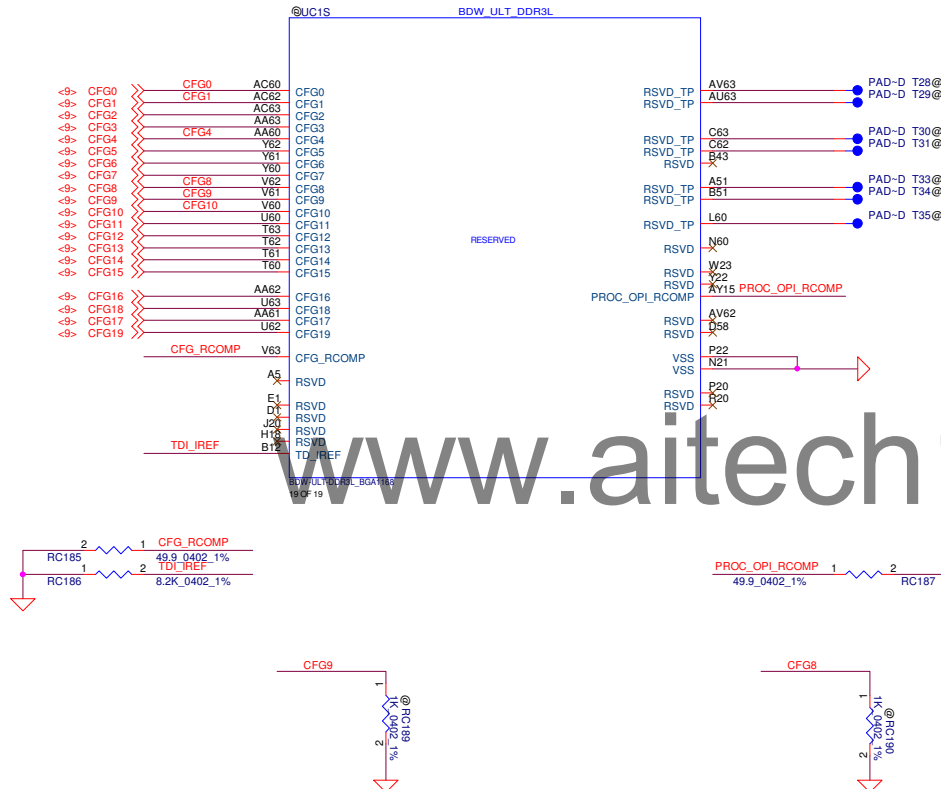


PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
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H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	NA

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## CFG STRAPS for CPU



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed

SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegrardless of the locking of the unit

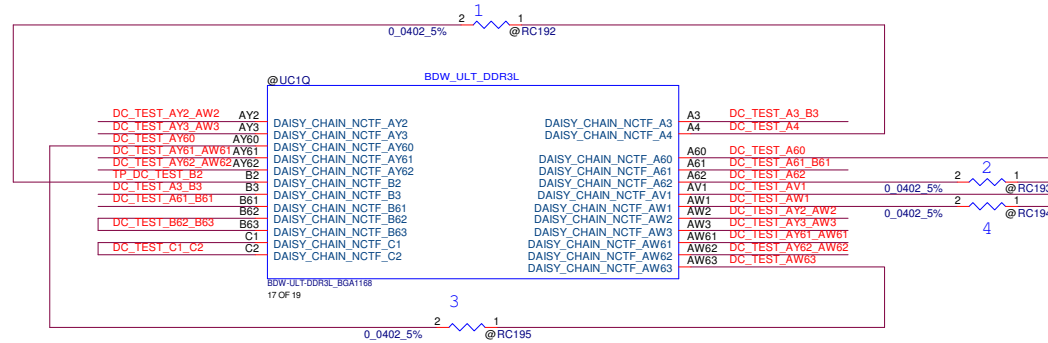
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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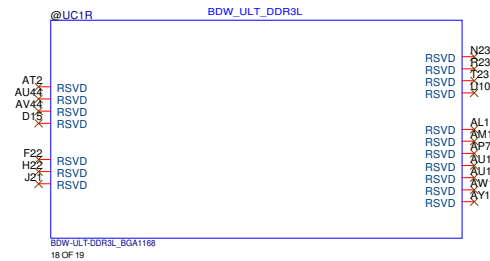
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#### Package Daisy Chain:

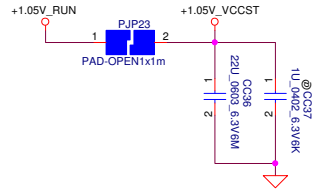
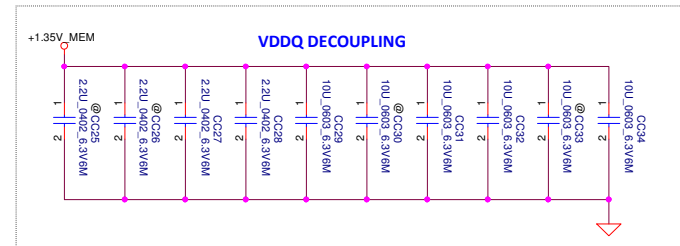
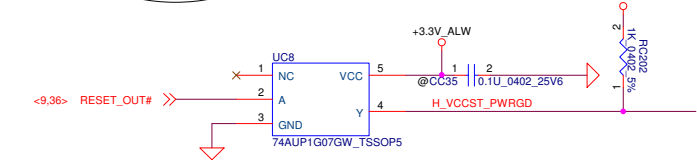
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- 3.AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
- 4.AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1

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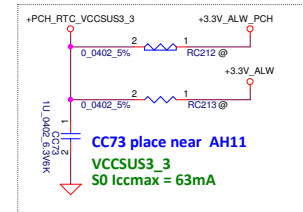
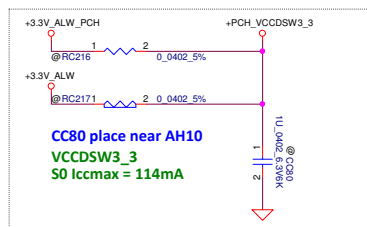


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CAD Note: RC209 SHOULD BE PLACED CLOSE TO CPU



Reminder below power rail need isolation for layout refer attach file for more detail that from Intel review feedback.

### Power Rail Isolation

Voltage Supply	Interface: (power rail isolation required)	PCH Pins sharing power rail
V1.05s	Core	J11, H11, H15, AE8, AF22
	OP1	AA21, W21
	HSIO	K9, L10, N8, P9, B18, B11, M9
	USB2	AG16, AG17
	CLKPLL	A20
	CLK(A)	R21, T21
	CLK(B)	J18, K19
V3.3 <sub>A</sub>	CLK(C)	J17
	GPIO	AC9, AA9, AE20, AE21
	RTC	AH11
V3.3 <sub>S</sub>	HDA	AH14
	GPIO	V8, W9
	SDIO	UB, T9
	Thermal Sensor	K14, K16

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CPU (11/12)

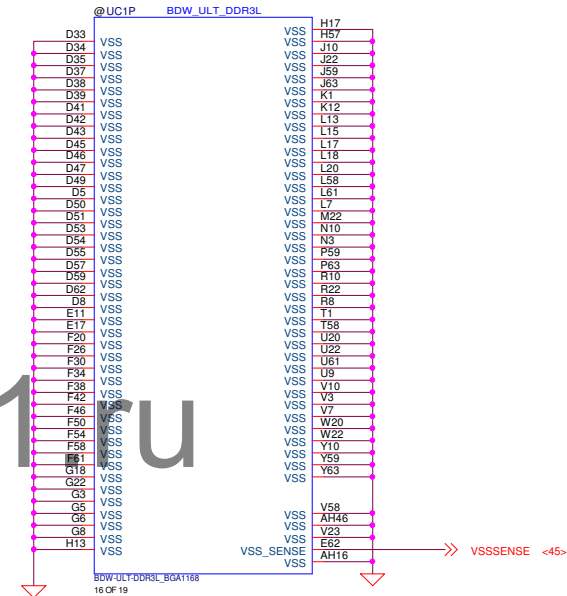
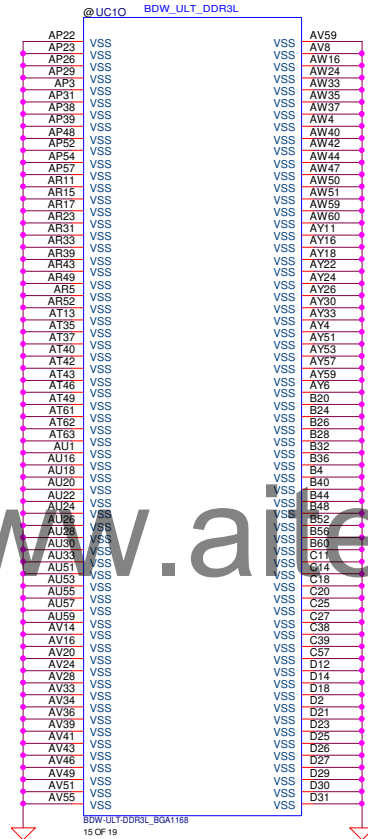
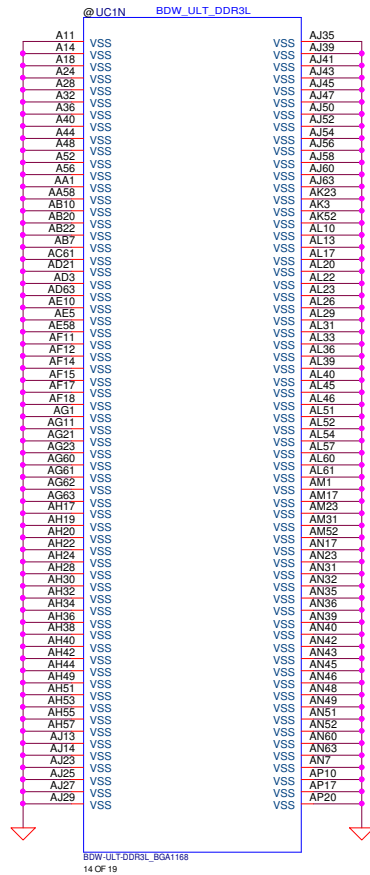
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VSS\_SENSE AH16



CAD Note: RC218 SHOULD BE PLACED CLOSE TO CPU

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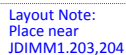
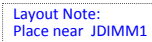
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**Compal Electronics, Inc.**

**CPU (12/12)**

**LA-A901P**

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## DDR3L

**I A-A901P**

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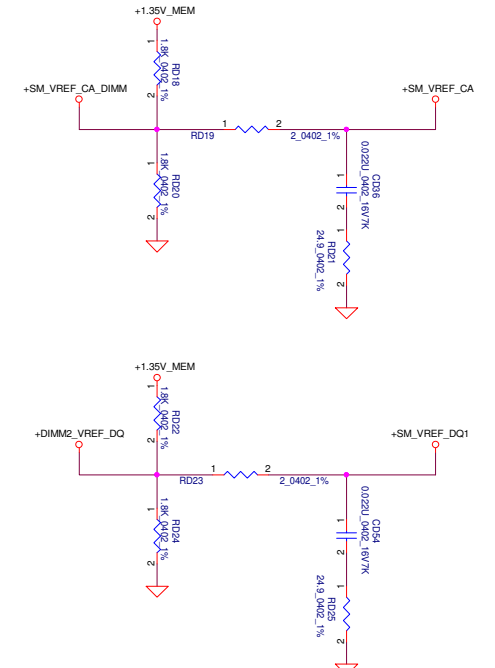
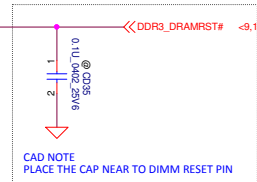
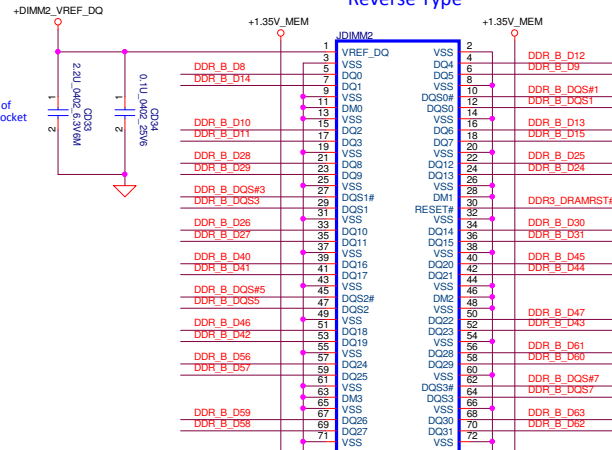


H=4mm  
Reverse Type

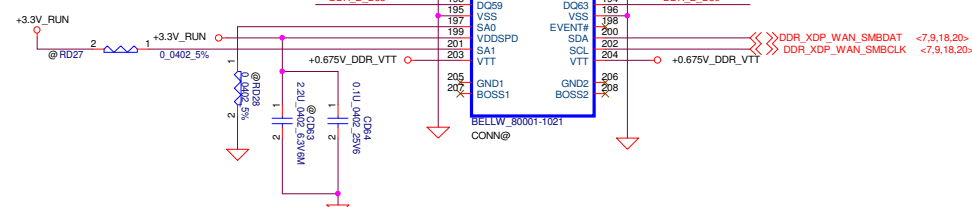
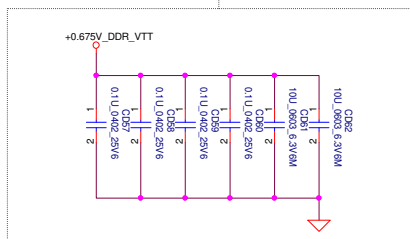
<8> DDR\_B\_DQS#(0..7) <<>  
<8> DDR\_B\_DQ(0..63) <<>  
<8> DDR\_B\_DQS(0..7) <<>  
<8> DDR\_B\_MA(0..15) <<>

Layout Note:  
Place near JDIMM2

Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket

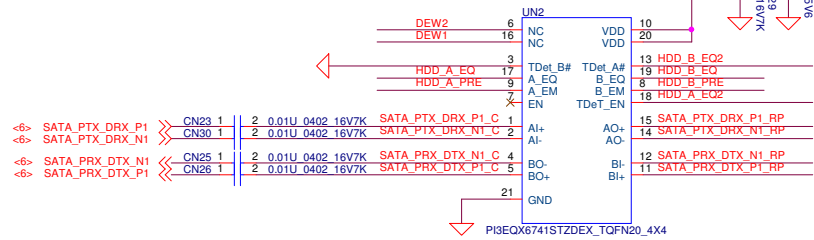


Layout Note:  
Place near  
JDIMM2.203,204



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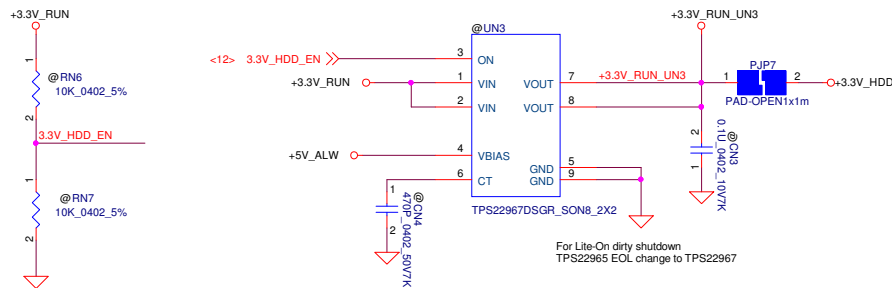
## SATA Repeater



	DEW2 PIN6	HDD_B_PRE PIN8	HDD_A_PRE PIN9	HDD_B_EQ2 PIN13	DEW1 PIN16	HDD_A_EQ PIN17	HDD_A_EQ2 PIN18	HDD_B_EQ PIN19
Pericom PI3EQX6741ST	NC	PD (RN11)	NC (IF0)	PD (RN25)	NC	NC	PH (RN22)	PD (RN16)
TI SN75LVCP601	NC (IF0)	PD (RN11)	PD (RN9)	PD (RN25)	NC (IF0)	PD (RN13)	PD (RN23)	NC
Parade PS8527C	PD (RN19)	PD (RN11)	PH (RN8)	PD (RN25)	NC	NC	PH (RN22)	NC

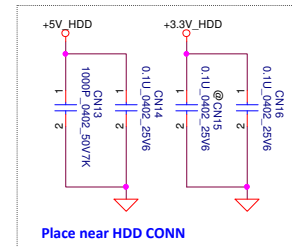
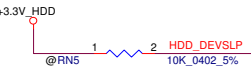
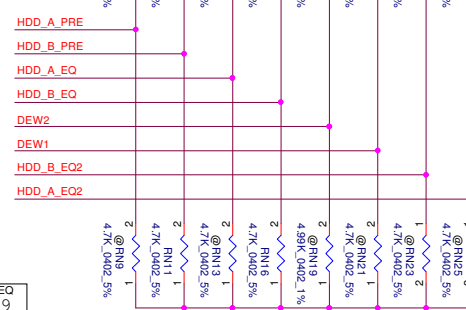
			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB
2nd	TI	0 NC 1	7dB 0dB 14dB	7dB 0dB 14dB	0 NC 1	0dB -6dB -3dB	0dB -6dB -3dB
3rd	Parade	EQ2 EQ1	A_EQ	B_EQ		A_EM	B_EM
		(M = VDD/2)					
		0 M	2.4dB	2.4dB	0		
		0 0	7.4dB	7.4dB	0		
		0 1	14.4dB	14.4dB	0		
		M M	12.2dB	12.2dB	M	-3.5dB	-3.5dB
		M 0	9.4dB	9.4dB	1	-1.5dB	-1.5dB
		M 1	13.3dB	13.3dB			
		1 M	6.2dB	6.2dB			
		1 0	11.2dB	11.2dB			
		1 1	5dB	5dB			

\* red color is current setting

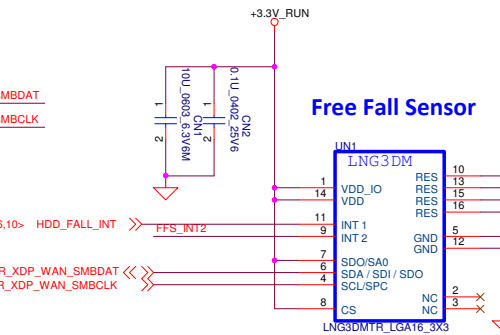
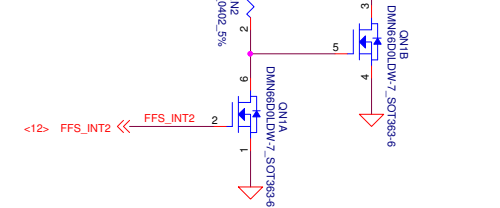


For Lite-On dirty shutdown  
TPS22965 EOL change to TPS22967

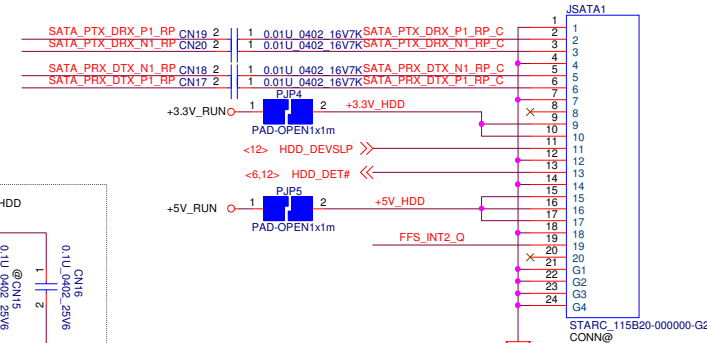
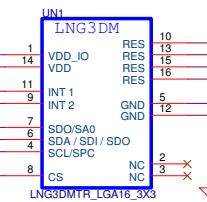
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Place near HDD CONN



## Free Fall Sensor

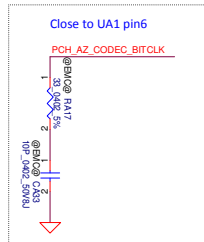
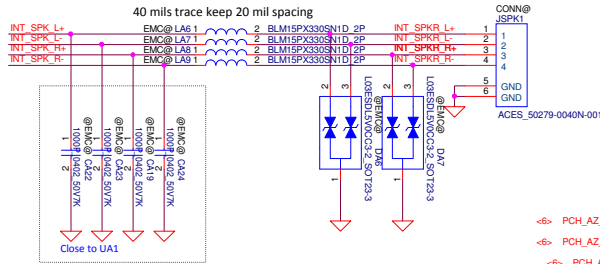


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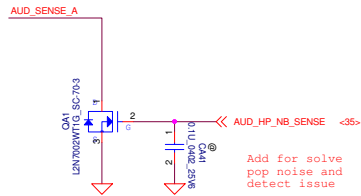
Compal Electronics, Inc.			
HDD CONN			
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1W x 1ch, 4ohm (Transducer spec is 80hm/0.5Watt per unit, there are two transducer units in one speaker box.)

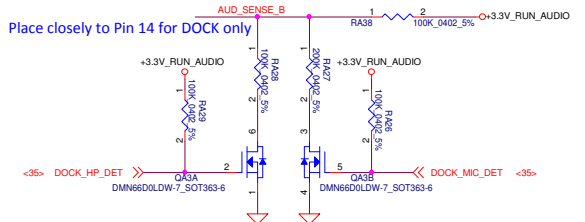
## Internal Speakers Header



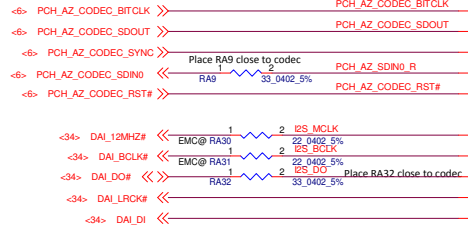
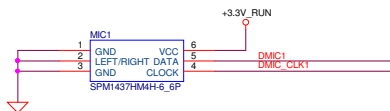
Place closely to Pin 13.



Place closely to Pin 14 for DOCK only

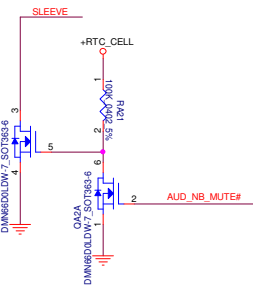
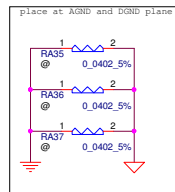


Digital Mic

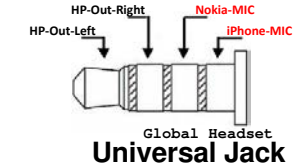
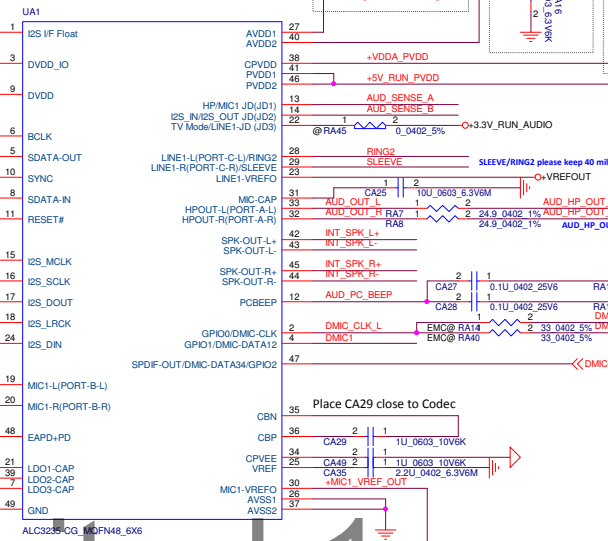


BCLK: Audio serial data bus bit clock input/output  
LRCLK: Audio serial data bus word clock input/output

AUD\_NB\_MUTE#



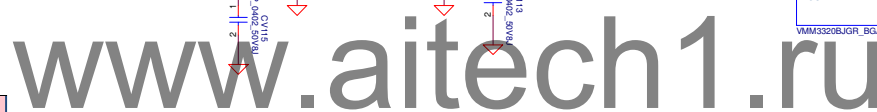
Realtek feedback  
Prevent the Noise from Combo Jack  
while system entry into S3 / S4 / S5



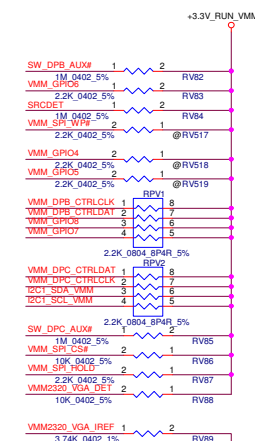
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Codec ALC3226			
Size			
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LA-A901P			
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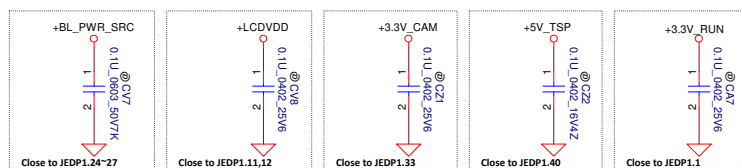
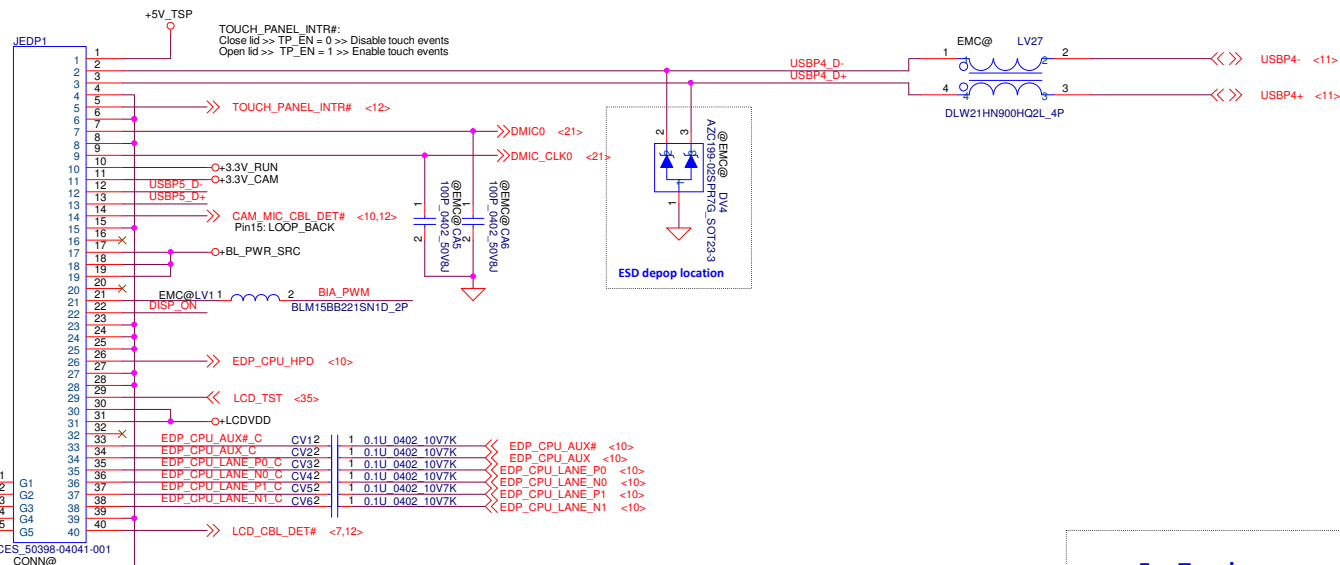


## Low Power Mode by external FET switch

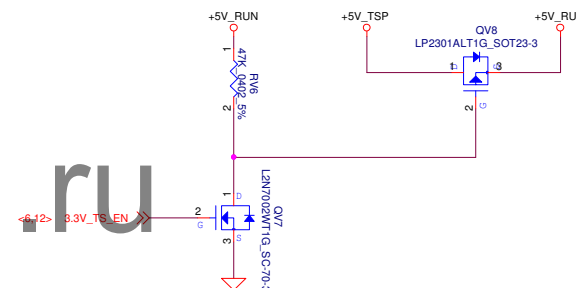


Title			
DP 1.2 MST HUB			
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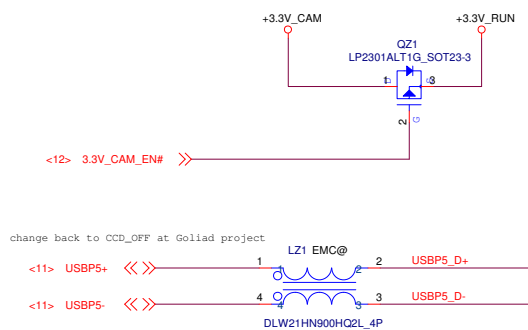
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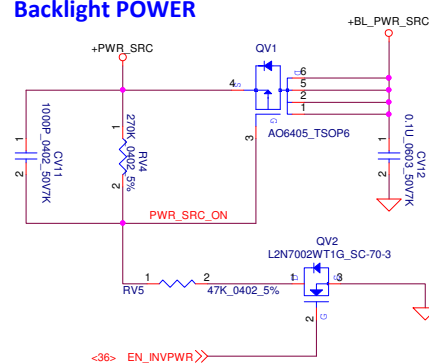
### For Touchscreen



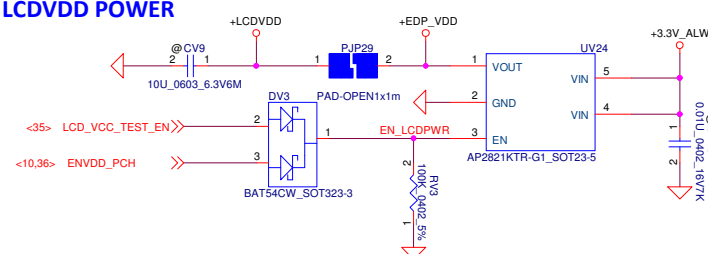
### WebCAM



### Backlight POWER



### LCDVDD POWER



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eDP CONN & Touch screen

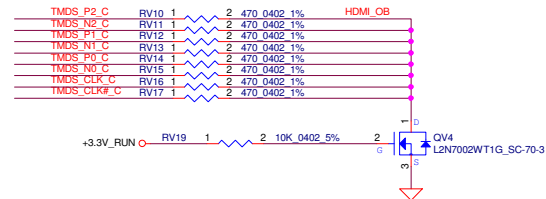
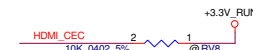
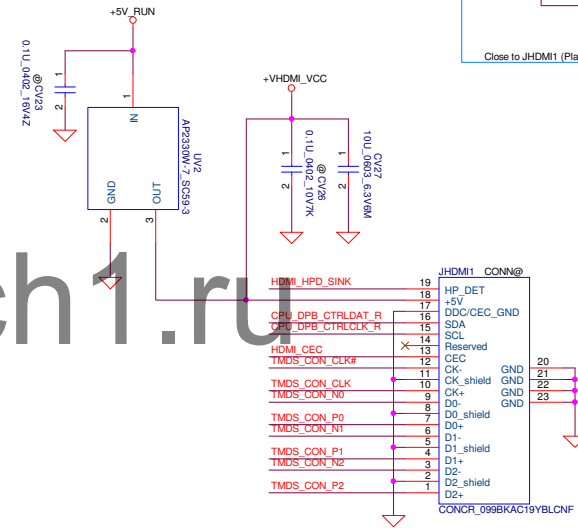
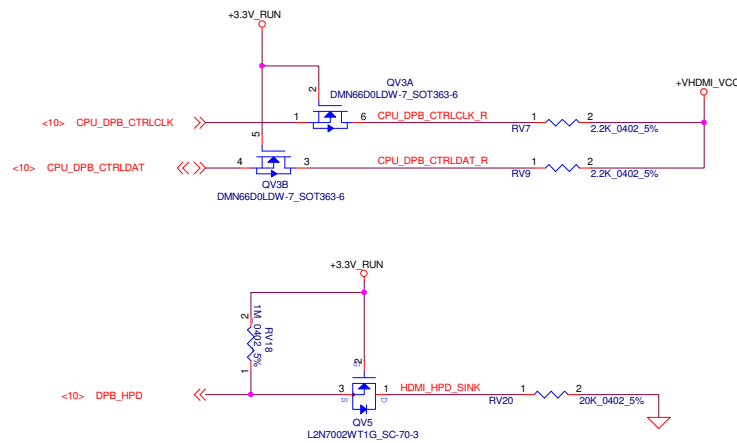
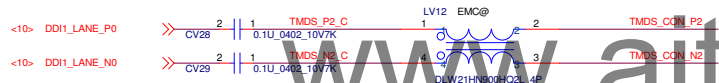
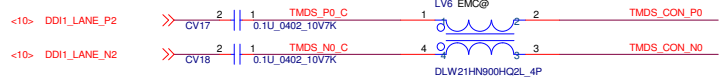
LA-A901P

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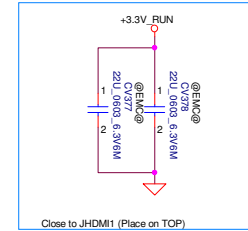
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# ESD Request



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HDMI CONN

LA-A901P

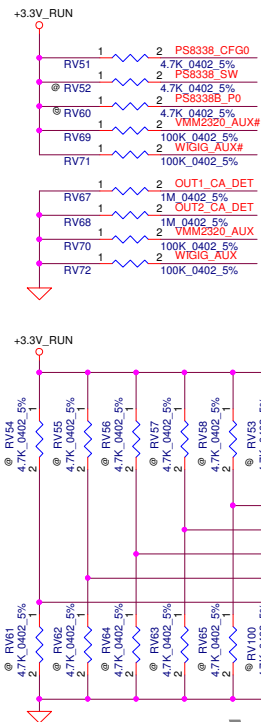
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PCB	DP SWITCH
H12 UMA	PS8338+PS8339
H12 Entry	PS8339
H14 DSC	PS8338
H14 UMA	PS8338
H14D_En	PS8338
H14U_En	PS8338
H15 DSC	PS8338
H15 UMA	PS8338
H15D_En	PS8338
H15U_En	PS8338



Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O  
For Control Switching Mode (CFG0 = L):  
SW = L: Port1 is selected (default)  
SW = H: Port2 is selected  
For Automatic Switching Mode (CFG0 = H):  
SW = L: Port1 has higher priority when both ports are plugged (default)  
SW = H: Port2 has higher priority when both ports are plugged

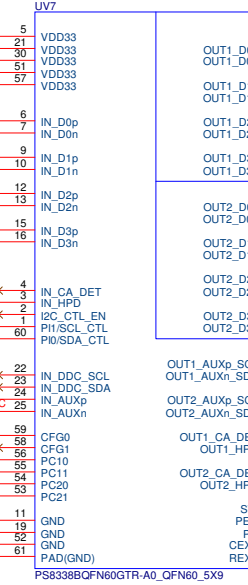
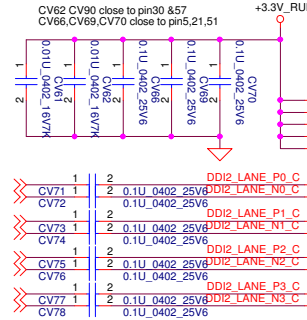
<10> DDI2\_LANE\_P0  
<10> DDI2\_LANE\_N0  
<10> DDI2\_LANE\_P1  
<10> DDI2\_LANE\_N1  
<10> DDI2\_LANE\_P2  
<10> DDI2\_LANE\_N2  
<10> DDI2\_LANE\_P3  
<10> DDI2\_LANE\_N3

<10> CPU\_DPC\_AUX  
<10> CPU\_DPC\_AUX#

for support TMDS signal need contact SCL/SDA to P22.23  
CPU\_DPC\_AUX  
CPU\_DPC\_AUX#

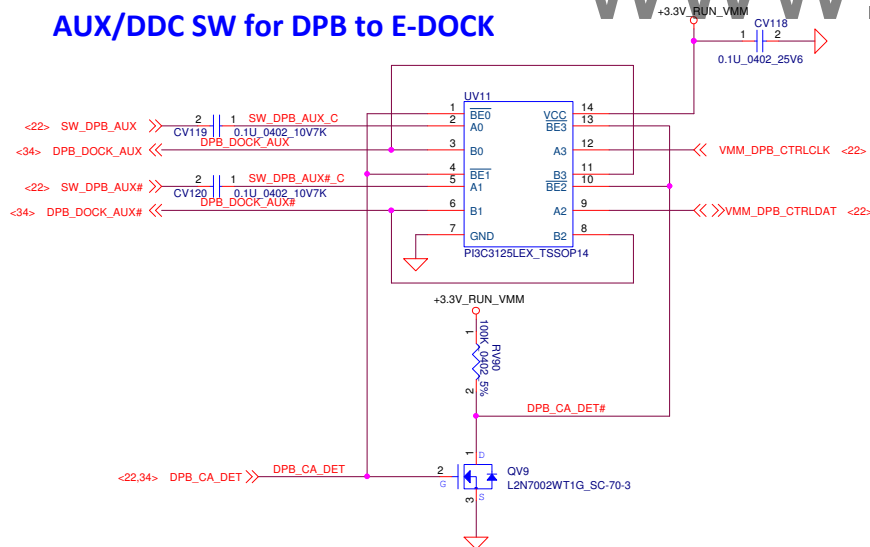
PS8338B\_P1  
PS8338B\_PC10  
PS8338B\_PC11  
PS8338B\_PC20  
PS8338B\_PC21  
PS8338B\_PEQ

Dock has high priority when both ports plugged

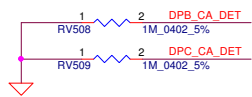
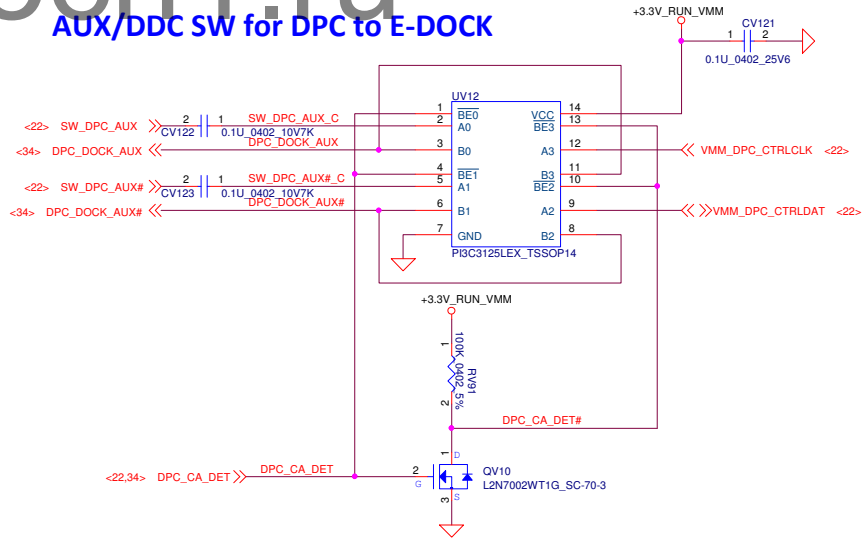


50 OUT1\_D0p >>> VMM2320\_P0 <22>  
49 OUT1\_D0n >>> VMM2320\_N0 <22>  
47 OUT1\_D1p >>> VMM2320\_P1 <22>  
46 OUT1\_D1n >>> VMM2320\_N1 <22>  
45 OUT1\_D2p >>> VMM2320\_P2 <22>  
44 OUT1\_D2n >>> VMM2320\_N2 <22>  
42 OUT1\_D3p >>> VMM2320\_P3 <22>  
41 OUT1\_D3n >>> VMM2320\_N3 <22>  
40 OUT2\_D0p >>> WIGIG\_LANE\_P0 <30>  
39 OUT2\_D0n >>> WIGIG\_LANE\_N0 <30>  
37 OUT2\_D1p >>> WIGIG\_LANE\_P1 <30>  
36 OUT2\_D1n >>> WIGIG\_LANE\_N1 <30>  
35 OUT2\_D2p >>> WIGIG\_LANE\_P2 <30>  
34 OUT2\_D2n >>> WIGIG\_LANE\_N2 <30>  
32 OUT2\_D3p >>> WIGIG\_LANE\_P3 <30>  
31 OUT2\_D3n >>> WIGIG\_LANE\_N3 <30>  
26 OUT1\_AUXp\_SCL >>> VMM2320\_AUX <22>  
27 OUT1\_AUXn\_SDA >>> VMM2320\_AUX# <22>  
28 OUT2\_AUXp\_SCL >>> WIGIG\_AUX <30>  
29 OUT2\_AUXn\_SDA >>> WIGIG\_AUX# <30>  
43 OUT1\_CA\_DET >>> VMM2320\_HP\_D <22>  
48 OUT1\_HP\_D >>> VMM2320\_HP\_D <22>  
33 OUT2\_CA\_DET >>> WIGIG\_HP\_D <30>  
38 OUT2\_HP\_D >>> WIGIG\_HP\_D <30>  
18 PS8338B\_SW >>> PS8338B\_PEQ  
14 PS8338B\_PEQ >>> PS8338B\_PEQ

## AUX/DDC SW for DPB to E-DOCK



## AUX/DDC SW for DPC to E-DOCK



	DP	HDMI
DPB_CA_DET	0	1
DPC_CA_DET	0	1

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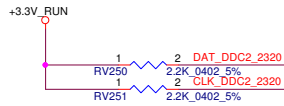
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DP SW			
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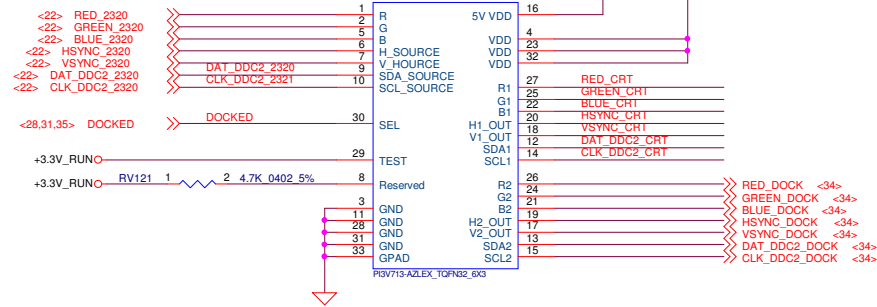
## VGA SW

PCB	VGA SWITCH
H12 UMA	NA
H12 Entry	NA
H14 DSC	PI3V713
H14 UMA	PI3V713
H14D_En	NA
H14U_En	NA
H15 DSC	PI3V713
H15 UMA	PI3V713
H15D_En	NA
H15U_En	NA

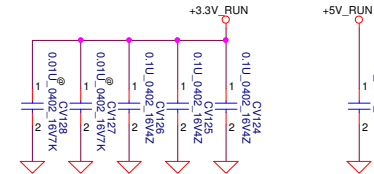


source from VMM2320

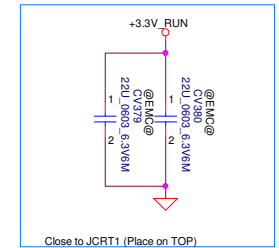
## VGA SW for MB/DOCK



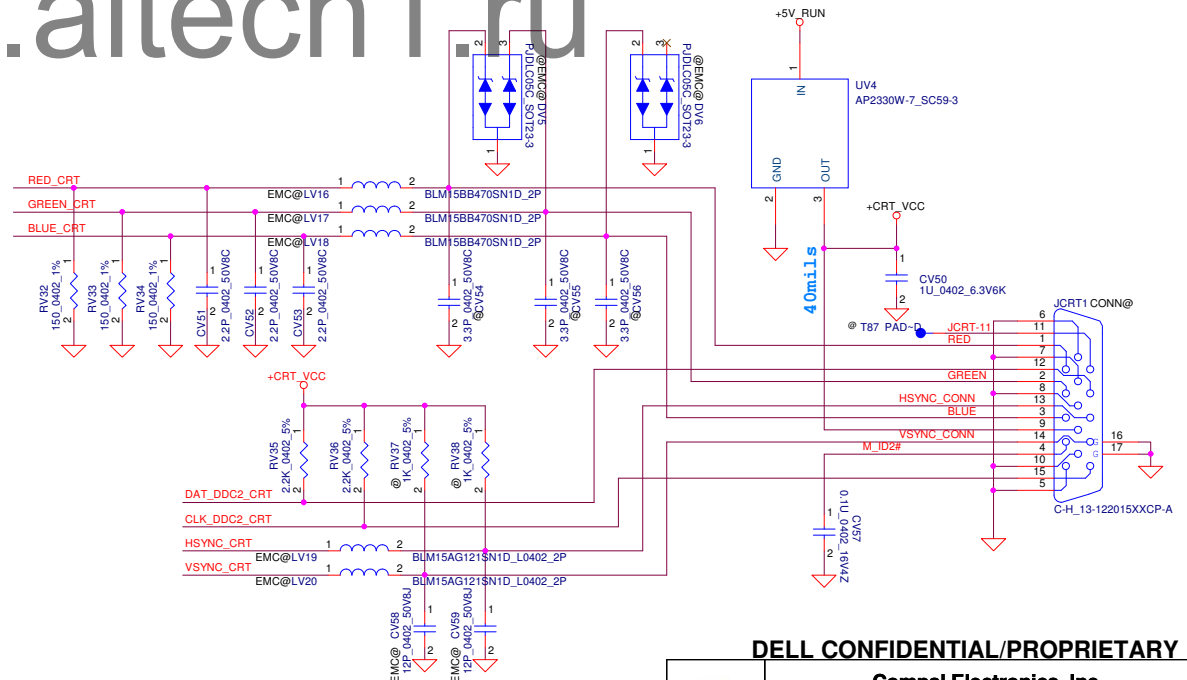
SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



## ESD Request



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Title		
VGA SW & VGA Conn		
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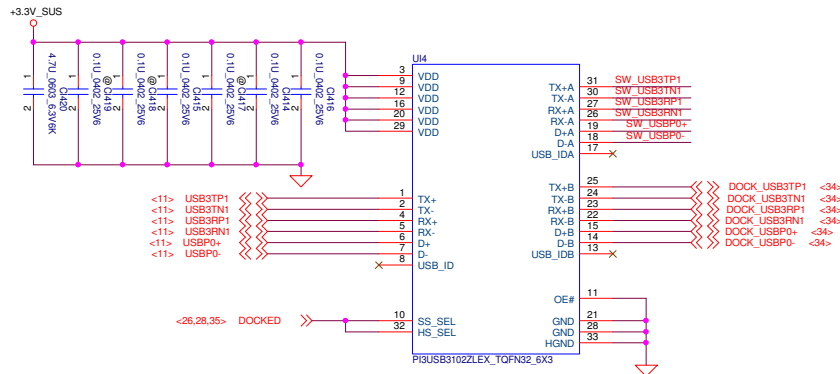
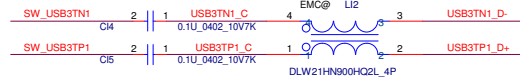
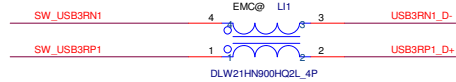
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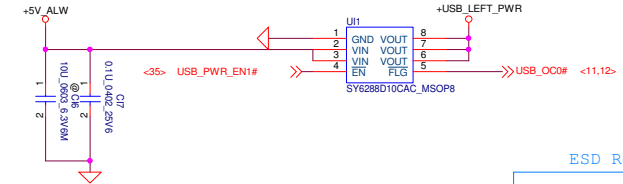
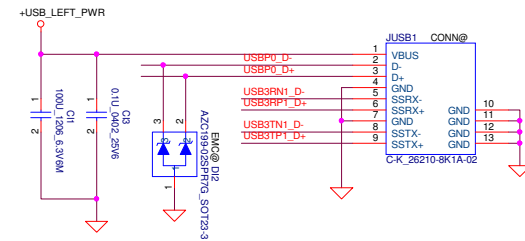
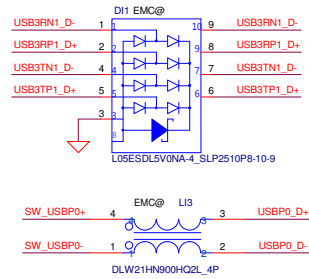




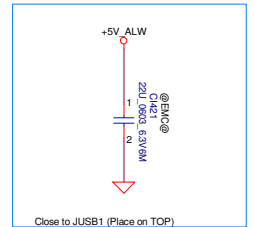


check port mapping

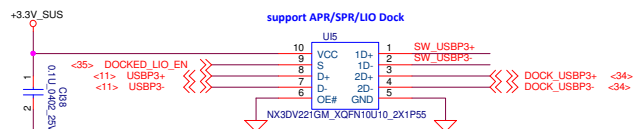
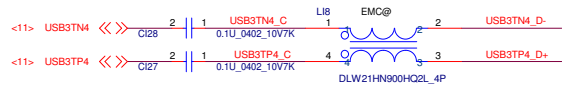
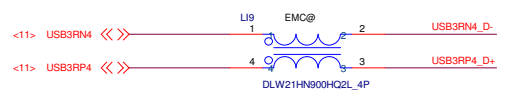
DOCKED	function
1	Dock
0	M/B



ESD Request

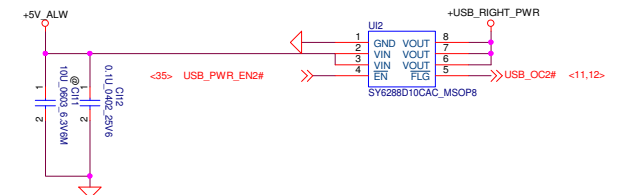
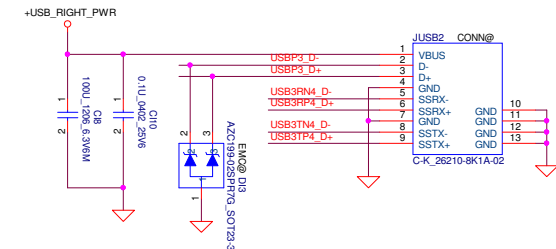
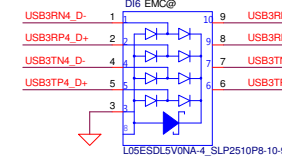


PCB	USB2 0	USB2 3
H12 UMA	USB3102	NX3DV221
H12 Entry	NA	NA
H14 DSC	USB3102	NX3DV221
H14 UMA	USB3102	NX3DV221
H14D_En	NA	NA
H14U_En	NA	NA
H15 DSC	USB3102	NX3DV221
H15 UMA	USB3102	NX3DV221
H15D_En	NA	NA
H15U_En	NA	NA



check port mapping

DOCKED_LIO_EN	function
1	Dock
0	M/B



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Houston 14 support NFC on USH

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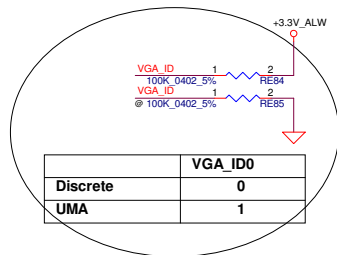
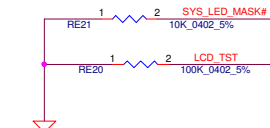
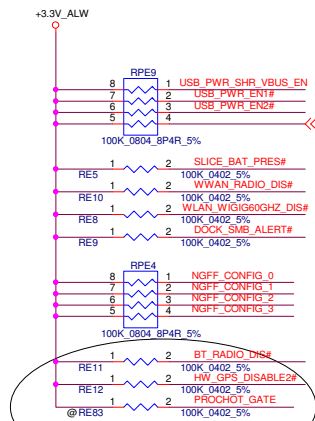


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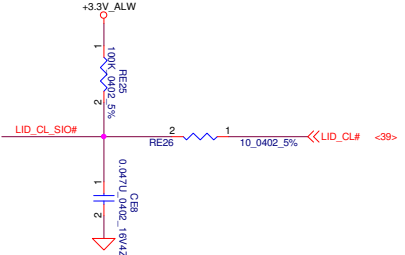
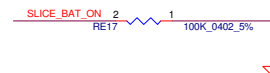
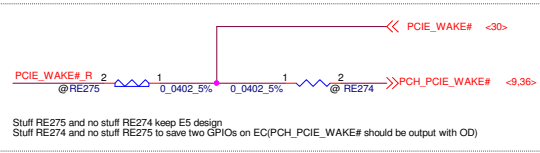
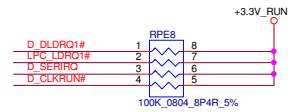
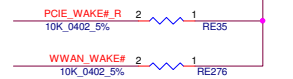
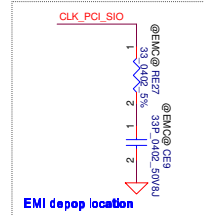
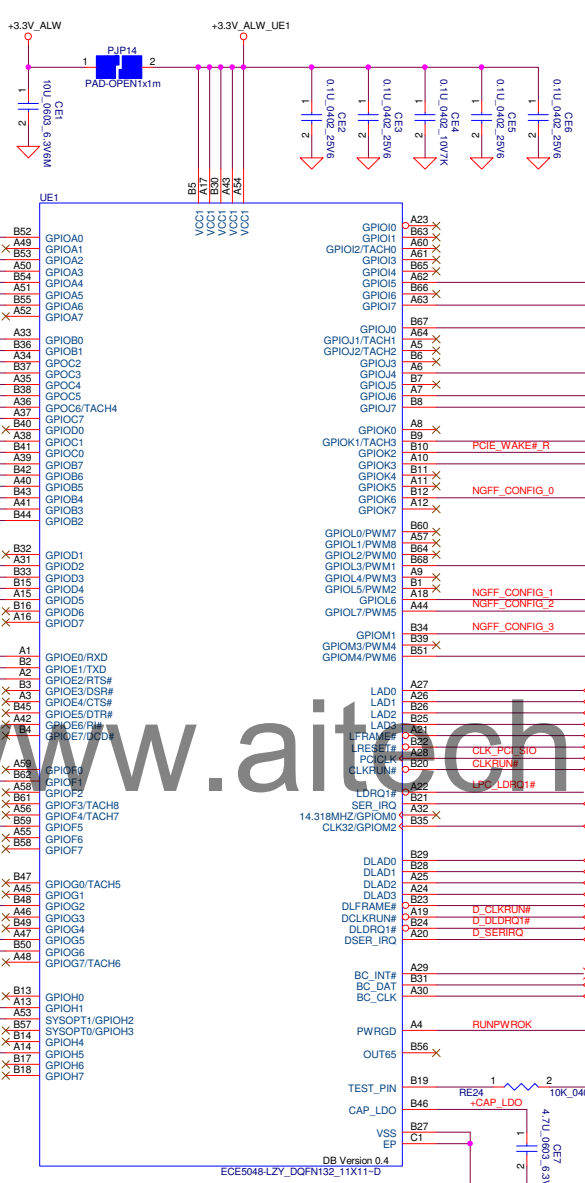
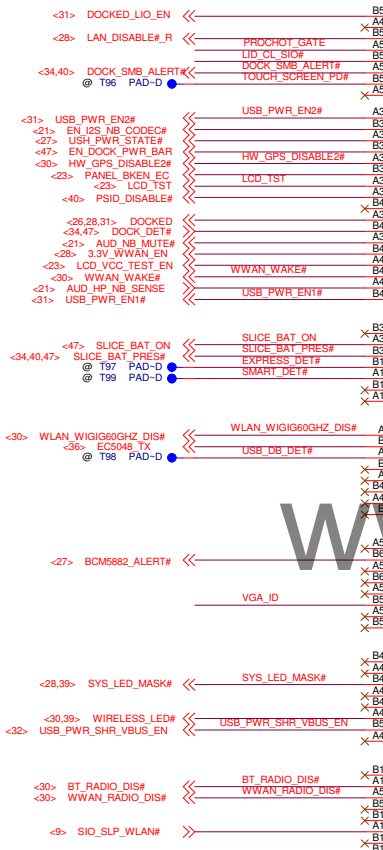
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VGA_ID0	
Discrete	0
UMA	1



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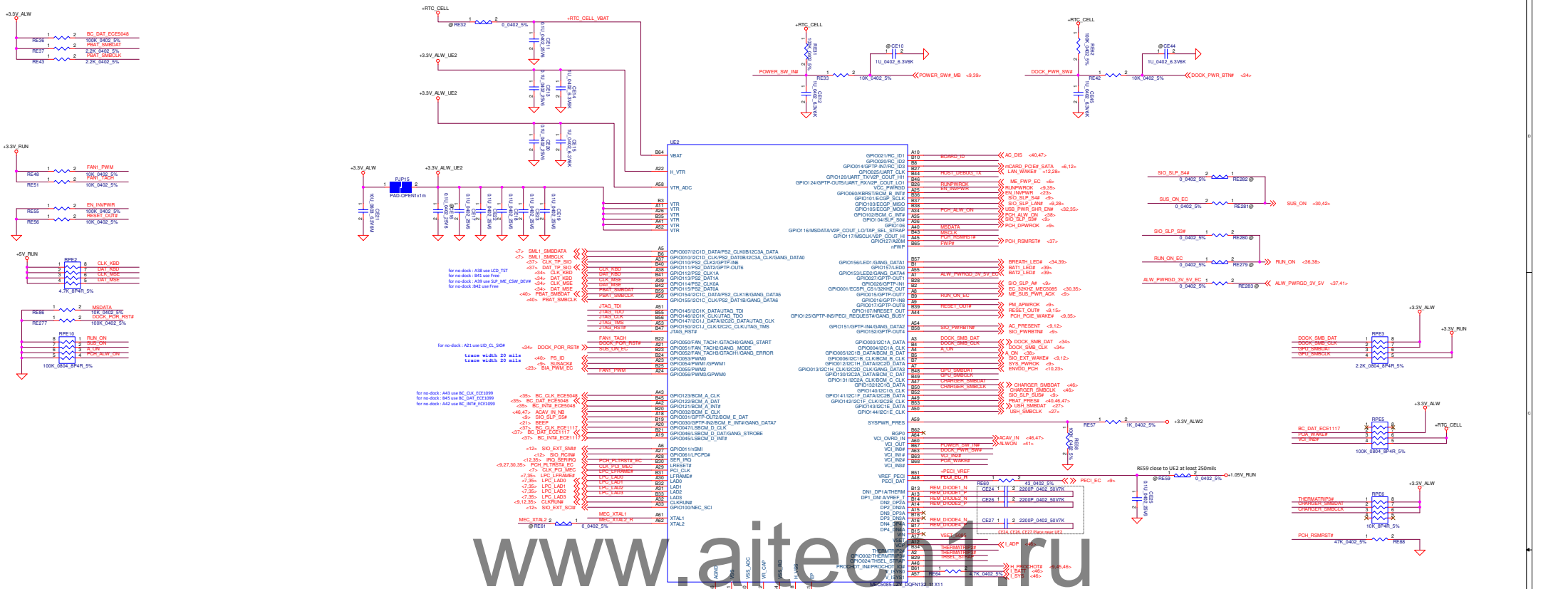
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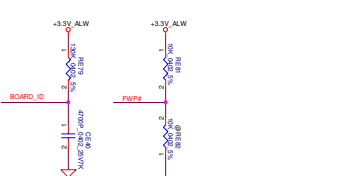
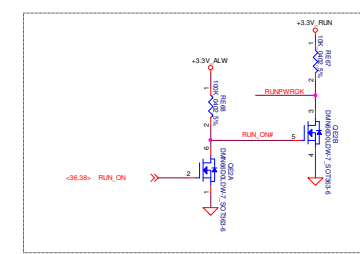
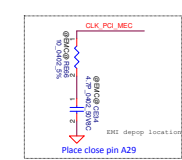
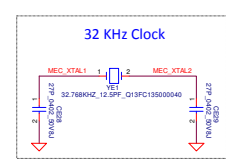
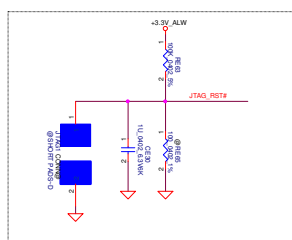


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### Setting for Thermal Design

5085 Channel	Location
DP1/DN1	CPU
DP2/DN2	DIMM
DN2a/DP2a	WiGig
DP4/DN4	V.R

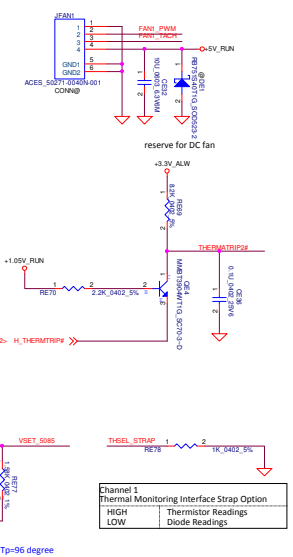
Place under CPU  
Place CE35 close to the QE3 as possible

DP2/DN2 for SODIMM on QE5, place QE5 close to SODIMM and CE37 close to QE5

DN2a/DP2a for WiGig on QE7, place QE7 close to WiGig and CE46 close to QE7

DP4/DN4 for skin on QE6, place QE6 close to Vcore VR choke.

Rest=1.58K, Tp=96 degree



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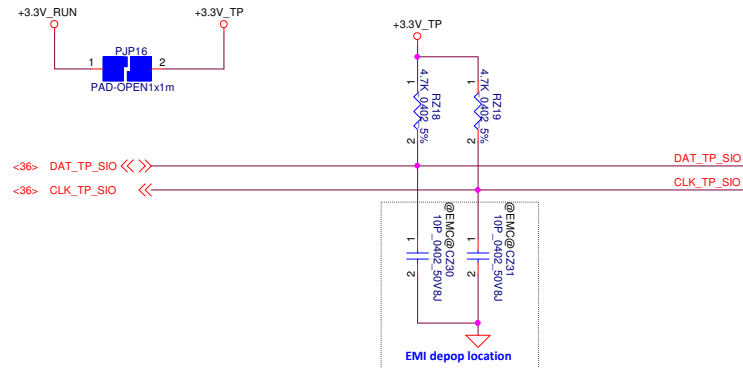
MEC5085

Document Number

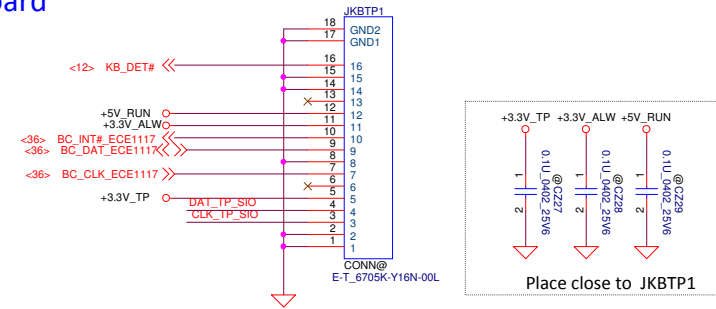
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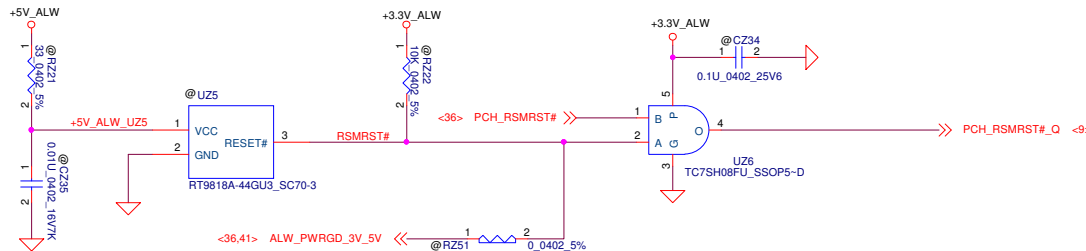
## Touch Pad



## Keyboard



## RSMRST circuit



### @eDP Cable W CAM

Part Number	Description
DC02C007600	H-CONN SET 13D MB-EDP-CAMERA

### @eDP TS Cable W CAM

Part Number	Description
DC02C007C00	H-CONN SET 13D MB-EDP-CAMERA-TS

### @eDP Cable W/O CAM

Part Number	Description
DC02C007D00	H-CONN SET 13D MB-EDP

### @SATA SPINDLE Cable

Part Number	Description
DC02C007500	H-CONN SET 13D MB-SPINDLE HDD

### @SATA Cable

Part Number	Description
DC02C007400	H-CONN SET 13D MB-MSATA HDD

### @DC-IN Cable

Part Number	Description
DC301000100	CONN SET 13P DCJACK-MB 20W1003-041110F

### @BATT Cable

Part Number	Description
DC02001X800	H-CONN SET 13D MB-BATT CABLE

### @LED FFC

Part Number	Description
NBX0001JG00	FFC 10P F P0.5 PAD0.3 172MM MB-LED/B 13D

### @FP FFC

Part Number	Description
NBX0001JK00	FFC 8P F P0.5 PAD.3 123MM MB-FP VALIDITY

### @TP FFC

Part Number	Description
NBX0001JJ00	FFC 16P F P0.5 PAD=0.3 119MM MB-TP 13D

### @USH Board FFC

Part Number	Description
NBX0001JJ00	FFC 26P G P0.5 PAD.3 88MM MB-USH/B 13D

### @RTC BATT

Part Number	Description
GC02001DS00	BATT CR2032 3V 225MAH PA 5 W/C 30MM

### @FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

### @Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

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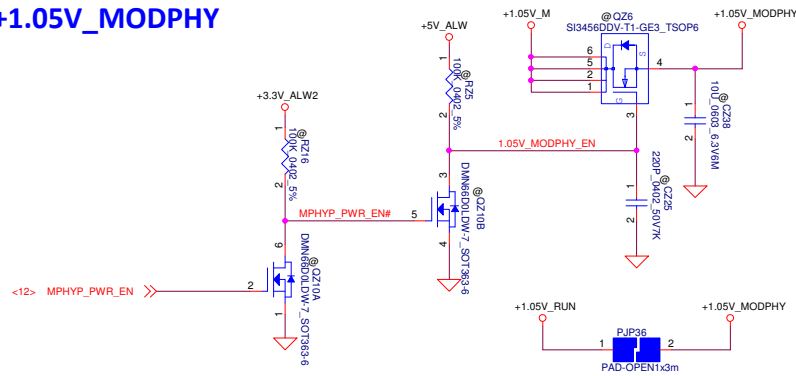
Keyboard

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Keyboard	LA-A901P	0.3
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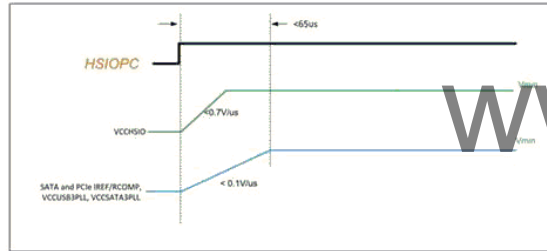
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## +1.05V\_MODPHY

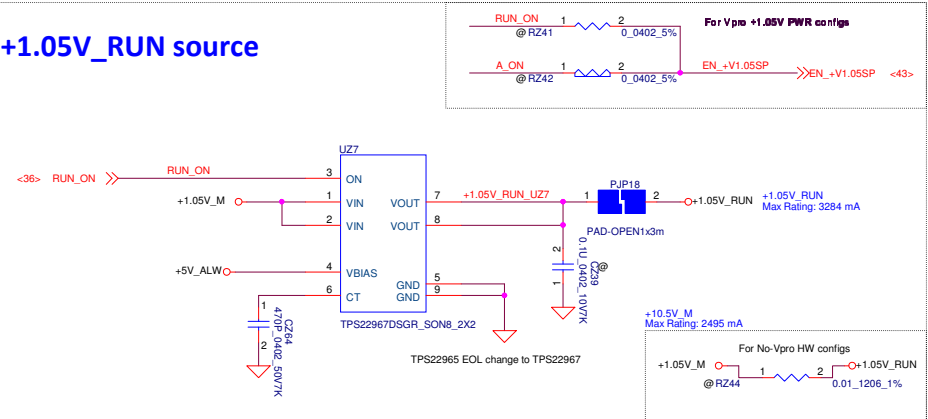


if support MODPHY off keep DSC solution  
MODPHY timing spec 0.7V/us and <65us

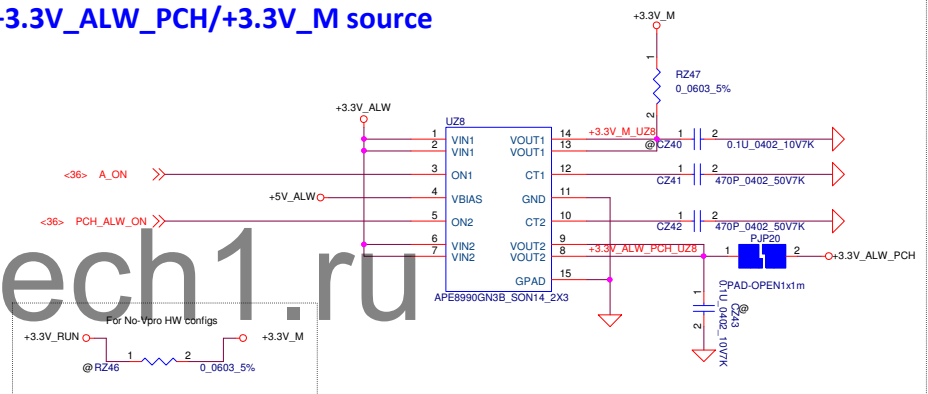
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



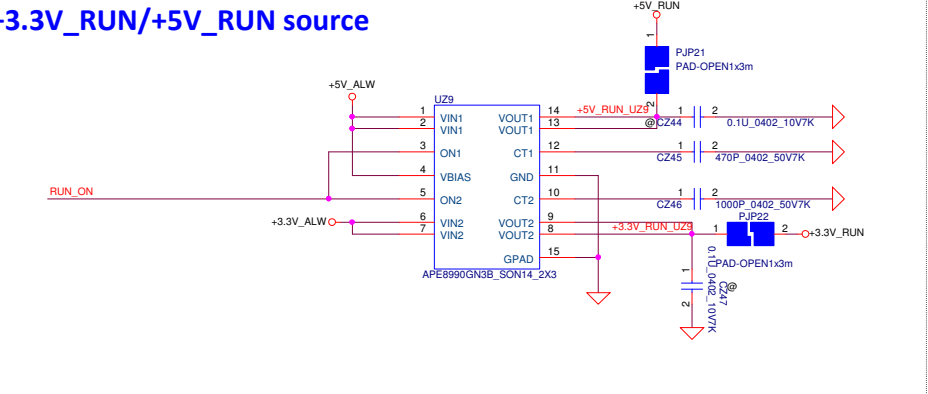
## +1.05V\_RUN source



## +3.3V\_ALW\_PCH/+3.3V\_M source



## +3.3V\_RUN/+5V\_RUN source



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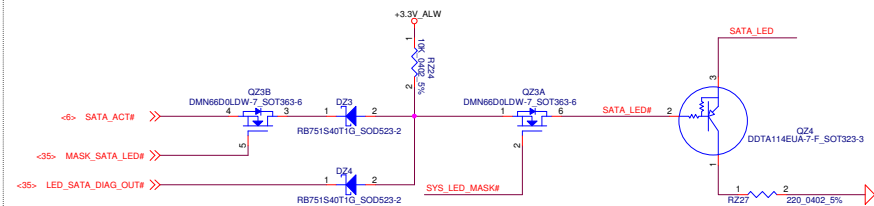
Power control

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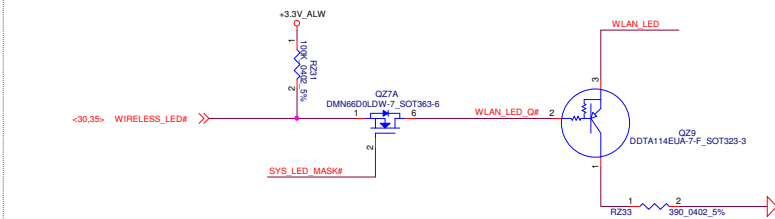
## HDD LED solution for White LED



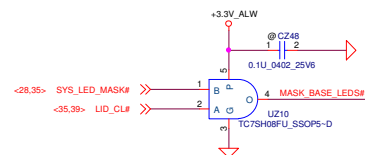
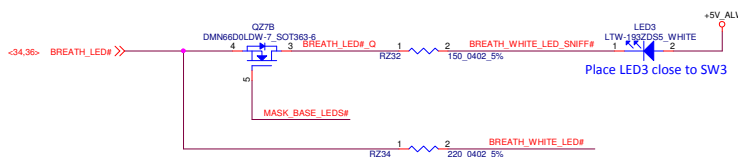
## Battery LED



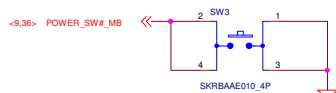
## WLAN LED solution for White LED



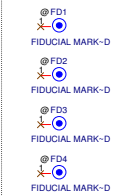
## Breath LED



## POWER & INSTANT ON SWITCH

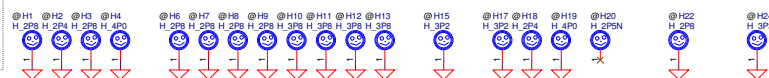


## Fiducial Mark

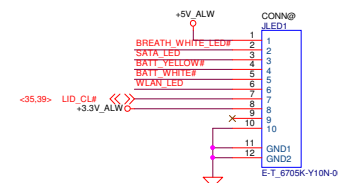


## LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



## LED board CONN

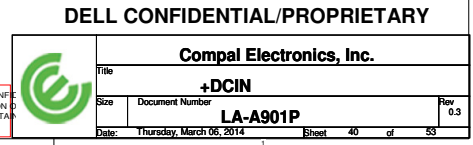


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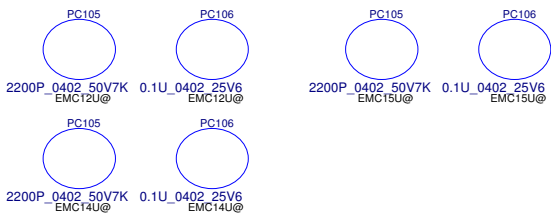
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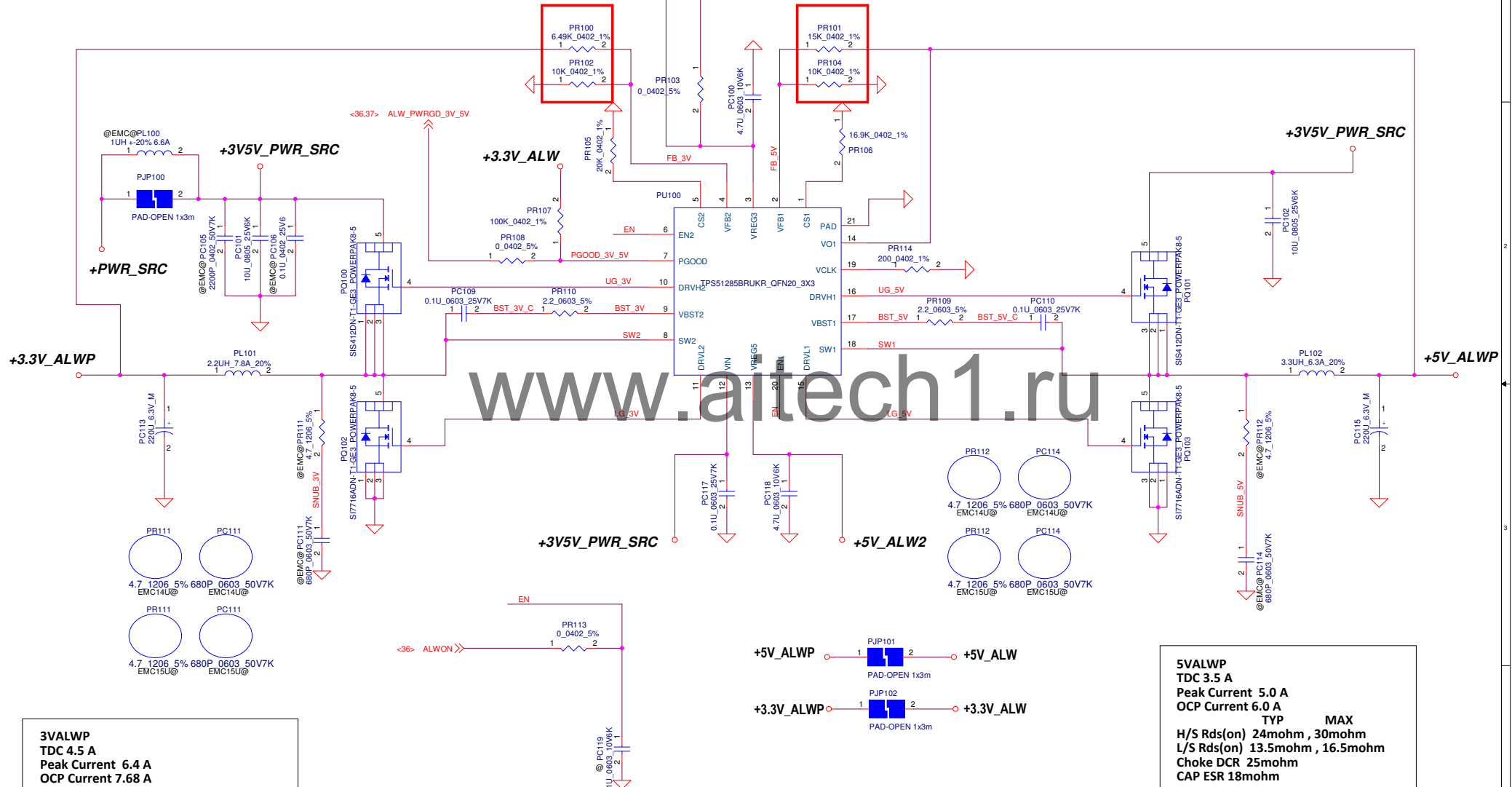


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# **+3.3V\_ALW2 +3.3V\_RTC\_LDO**



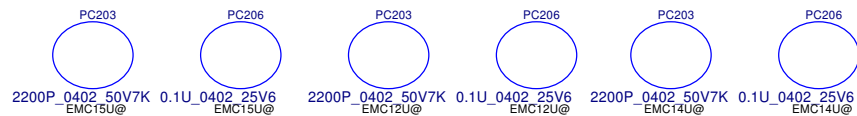
**3VALWP**  
 TDC 4.5 A  
 Peak Current 6.4 A  
 OCP Current 7.68 A  
 TYP MAX  
 H/S Rds(on) 24mohm , 30mohm  
 L/S Rds(on) 13.5mohm , 16.5mohm  
 Choke DCR 15.5mohm  
 CAP ESR 18mohm

**5VALWP**  
 TDC 3.5 A  
 Peak Current 5.0 A  
 OCP Current 6.0 A  
 TYP MAX  
 H/S Rds(on) 24mohm , 30mohm  
 L/S Rds(on) 13.5mohm , 16.5mohm  
 Choke DCR 25mohm  
 CAP ESR 18mohm

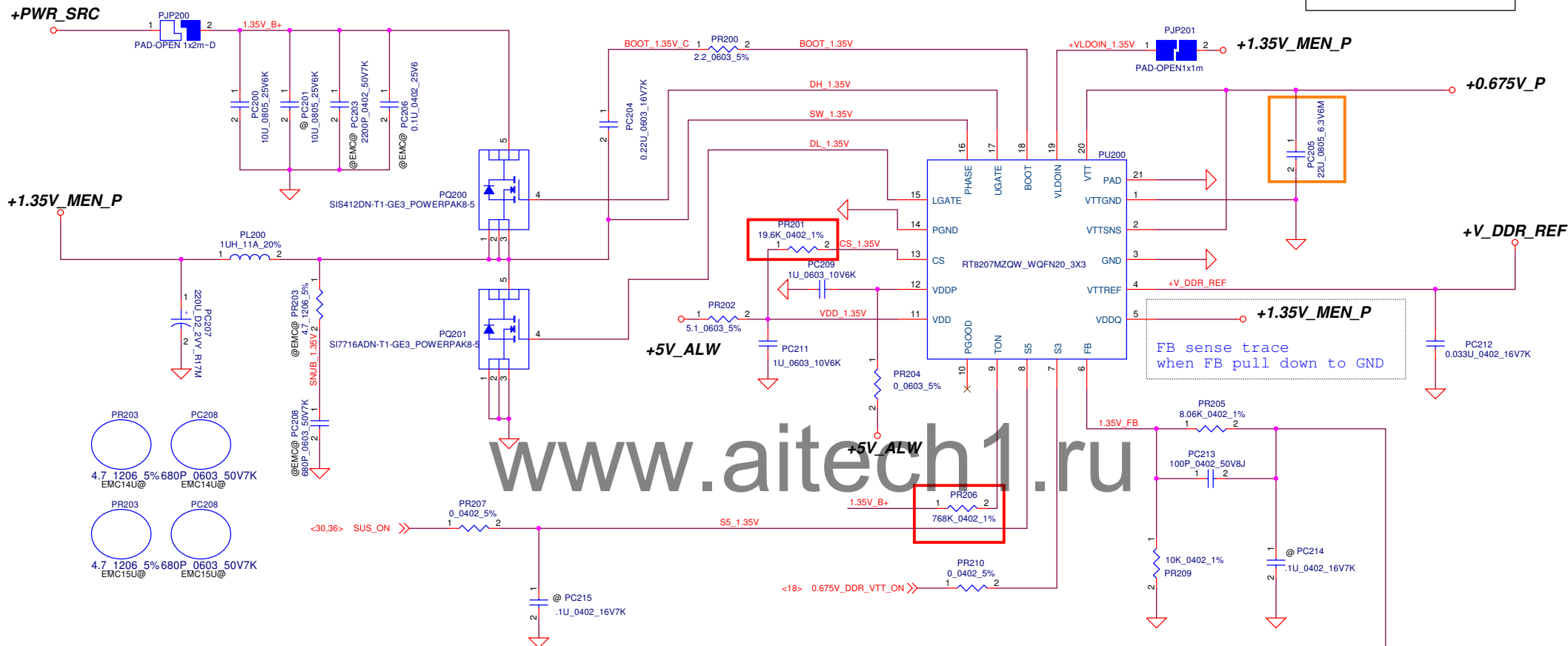
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<b>+5V_ALW/3.3V_ALW</b>			
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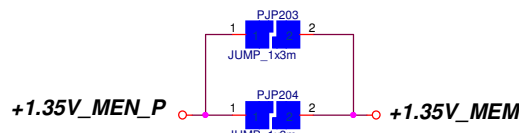


0.675Volt +/- 5%  
TDC 0.7 A  
Peak Current 1.0 A  
OCP Current 2.6 A fix by IC



Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off
S0	H	H	on	on	on

**+1.35V\_MEM**  
TDC 6.6 A  
Peak Current 9.5 A  
OCP Current 11.4 A  
TYP MAX  
H/S Rds(on) 24mohm, 30mohm  
L/S Rds(on) 13.5mohm, 16.5mohm  
Choke DCR 7.4mohm  
CAP ESR 17mohm



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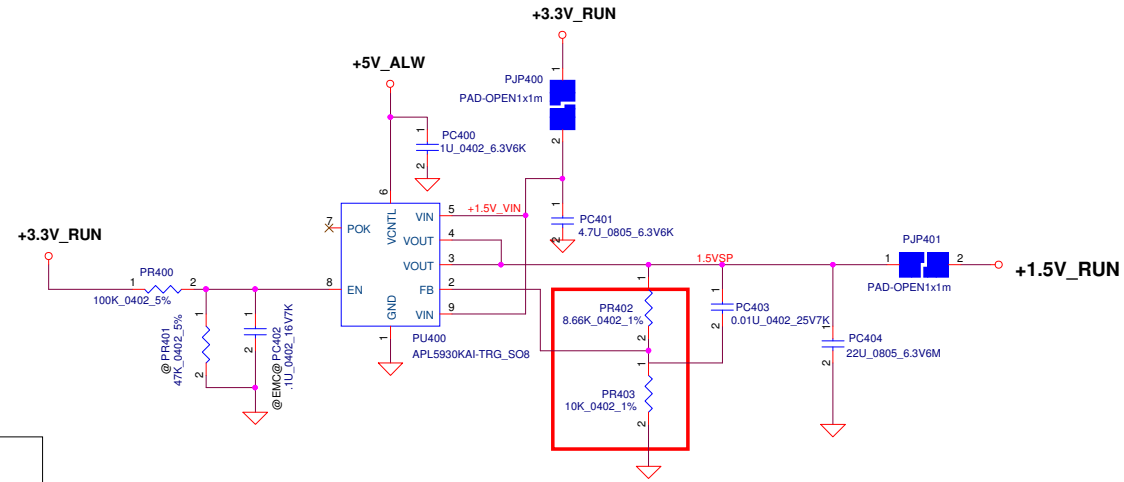
Title  
**+1.35V MEN/+0.675V DDR VTT**

Size Document Number  
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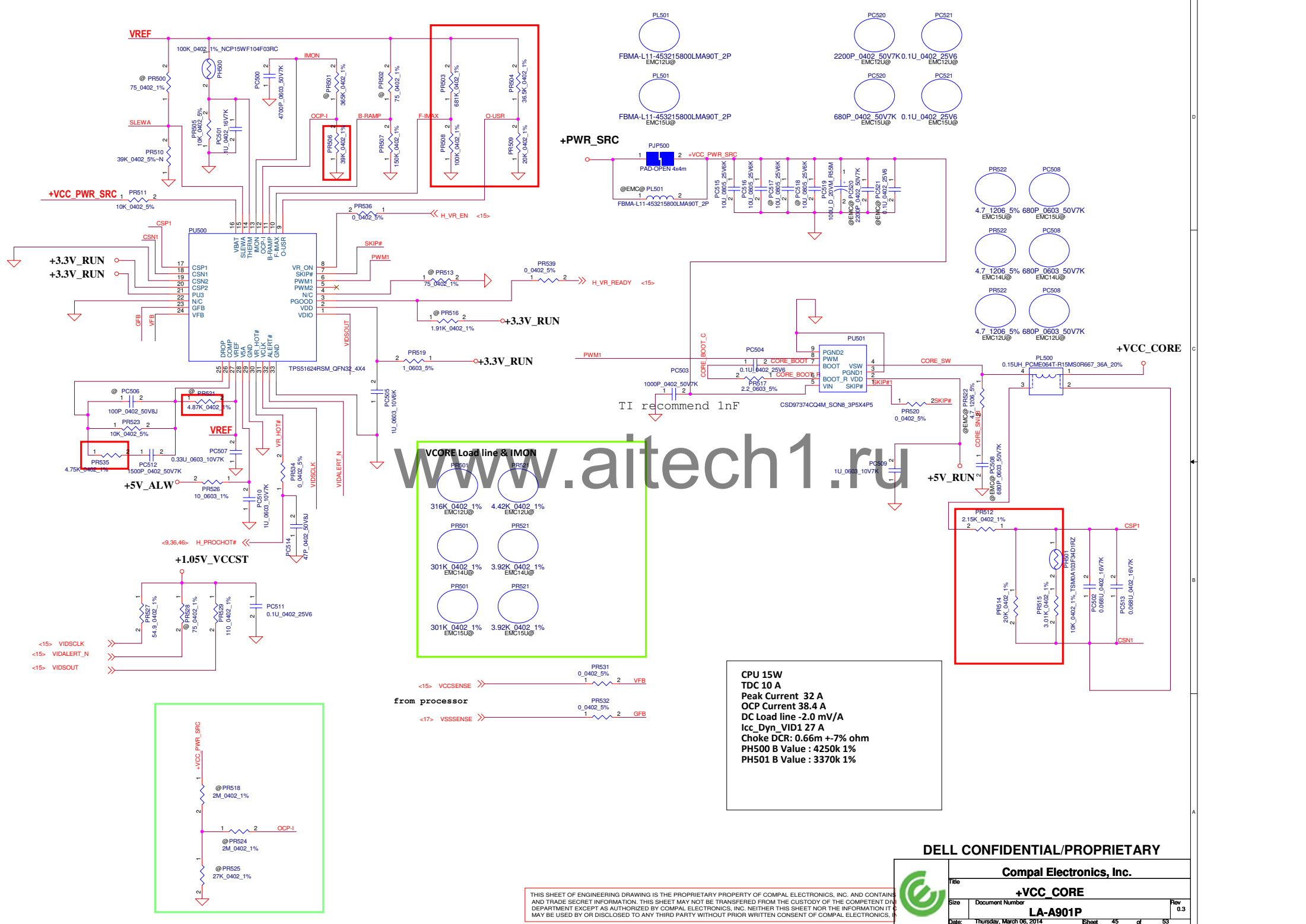


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CPU 15W  
TDC 10 A  
Peak Current 32 A  
OCP Current 38.4 A  
DC Load line -2.0 mV/A  
Icc\_Dyn\_VID1 27 A  
Choke DCR: 0.66m +/-7% ohm  
PH500 B Value : 4250k 1%  
PH501 B Value : 3370k 1%

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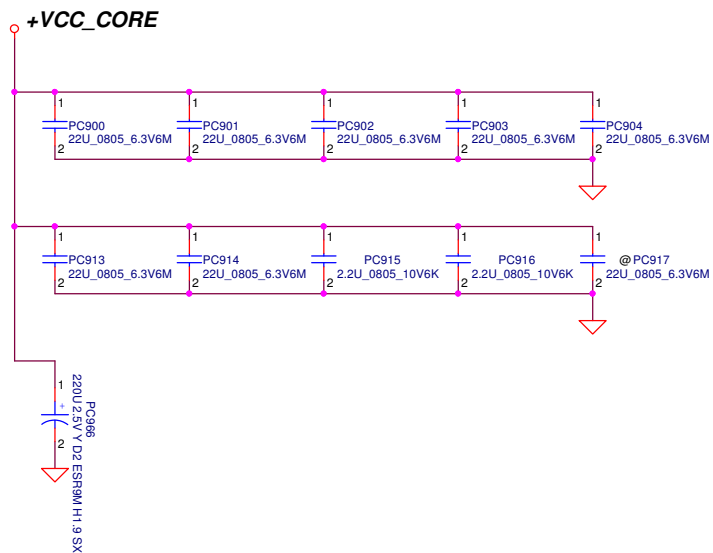
+VCC\_CORE

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### Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
B 1	47	Selector	10/8	Compal	Remove slice battery support circuit	Remove PC808, PC811, PC812 , PC814, PD806, PD807, PD811, PD814, PD819, PD821, PQ801, PQ807, PQ809, PQ811, PQ812, PQ818, PQ821, PQ828, PQ830, PQ831, PR802, PR804, PR808, PR813, PR815, PR816, PR817, PR821, PR823, PR825, PR834, PR836, PR837, PR839, PR849, PR852, PR861, PU805, PU807, PU808	X01
2	45	VCC_CORE	10/8	Compal	To prevent acoustic noise issue	Remove PC923, PC924, PC925, PC926, PC927, PC928, PC929, PC930, PC931, PC940, PC941, PC943, PC946, PC947, PC948 Add PC966	X01
3	42	1.35V_MEN	10/8	RICHTEK	To prevent IC damage	Add PR204	X01
4	46	Charger	10/8	Compal	Fine tune divider voltage	Change PR713, PR725 to 100k Change PR715, PR729 to 154k	X01
C 5	41, 43, 44	+1.05V_M +1.5V_RUN +3V/+5V	10/22	Compal	To improve the ability of anti-noise	Change PR307 to 7.5k Change PR310, PR102, PR104, PR403 to 10k Change PR100 to 6.49k Change PR101 to 15k Change PR402 to 8.66k	X01
6	46	Charger	10/25	Compal	Change /BATPRES pin control net from /BATPRES to PBAT_PRES#	Pop PR728 Depop PR816	X01
7	45	VCC_CORE	10/31	Compal	Fine tune IMON	Add PR518, PR524, PR525	X01
8	ALL	ALL	10/31	Compal	RF request	Add PC521, PC206, PC106, PC311, PC732 ( 0.1uF )	X01
9	ALL	ALL	10/31	Compal	RF request	Pop PR111,PC111,PR112,PC114,PR203,PC208,PR305,PC301,PR522,PC508, (4.7ohm, 680pF)	X01
B 10	46	Charger	10/31	Compal	To prevent VCP trigger PROCHOT#	PR703 change to 100ohm	X01
A							

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1	6	HW	2013/10/8	COMPAL	Follow intel reference circuit.	Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST	0.2 (X01)
2	27	HW	2013/10/8	COMPAL	Dell drop POA function.	Change JUSH1 from 26 pin to 20 pin, pin define follow E5	0.2 (X01)
3	36	HW	2013/10/8	COMPAL	Dell drop POA function.	remove POA_WAKE# off page symbol remove POA_ON/OFF#,make UE2.B62 to be NC pin	0.2 (X01)
4	22	HW	2013/10/9	COMPAL	IC version changed.	VMM2320 circuit change: 1. UV8 from VMM2320 change to VMM 2330 (SA00007G800) 2. UV8 pin J3, E5 to +1.05V_RUN 3. VMM_SPI_WP# reserved RV517, 2.2K resistor PU to +3.3V_RUN_VMM 4. VMM_GPIO4,reserved RV518, 2.2K resistor PU to +3.3V_RUN_VMM 5. VMM_GPIO5 reserved RV519, 2.2K resistor PU to +3.3V_RUN_VMM 6. add QV20,CZ69,RV210,RV212,QV21 external FET switch circuit 7. UV8 pin B5, B6 change to +3.3V_RUN_VMM 8. LP_CTL add RV516, 2.2K resistor PU to +3.3V_RUN_VMM 9. Depop RV73 10. add LP_EN on UV8.A5 (10/18) 11. depop QV20,CZ69,RV210,RV212, QV21 external FET switch circuit (10/24) 12.RPV2 pin1 & pin2 NC (11/4)	0.2 (X01)
5	23	HW	2013/10/9	COMPAL	Follow EMC suggestion	Change LI1,LI2,LI3,LI4,LI5,LI6,LI7,LI8,LI9,LV3,LV6,LV10,LV12,LV27 From SM070003K00 (S COM FI CHILISIN CMMI21T-900Y-N) To SM070003Y00 (S COM FI MURATA DLW21HN900HQ2L)	0.2 (X01)
6	9	HW	2013/10/9	COMPAL	reserved for S3 within 2s , system shutdown issue debug.	add RC26, , reserved RC27.	0.2 (X01)
7	36	HW	2013/10/9	COMPAL	board ID change.	RE79 change to 130K	0.2 (X01)
8	36	HW	2013/10/14	COMPAL	follow intel latest design guide.	pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor	0.2 (X01)
9	7	HW	2013/10/16	COMPAL	RF requirement.	add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)	0.2 (X01)
10	20,23,31,32	HW	2013/10/17	COMPAL	follow ESD recommend list.	change all ESD diode CPN change DI2, DI3, DI5, DV4 from SCA00001100(S ZEN ROW PJDLC05C 3P C/A SOT23) to SC600001600(S DIO ROW AZC199-02S.R7G C/C SOT23 ESD) change DI1,DI6,DI4 from SC300002800(S DIO(BR) TVWDF1004AD0 DFN ESD) to SC300002C00(S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD) change DA1,DA2,DA3,DA6,DA7 from SCA00001L00(S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD) to SCA00002900(S ZEN ROW L03ESDL5V0CC3-2 C/A SOT-23 ESD)	0.2 (X01)

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11	7,38	HW	2013/10/17	COMPAL	for UMA DOCK configure, it support has non-VPRO configure.	add PJP33, PJP34 UC3, CC7, RC50, RC55, RPC12, UZ7, CZ64 change to VPRO@	0.2 (X01)
12	38	HW	2013/10/17	COMPAL	power doesn't split VPRO & NPRO BOM.	add RZ41, RZ42, reserve it for VPRO & NVPRO option.	0.2 (X01)
13	39	HW	2013/10/17	COMPAL	SSI design will cause LED behavior error.	remove QZ5, QZ7.2 & QZ3.2 change to SYS_LED_MASK#	0.2 (X01)
14	20	HW	2013/10/17	COMPAL	To solve Line-on HDD dirty shut down issue.	add UN3, CN3, CN4, PJP7 and reserved it.	0.2 (X01)
15	30,36	HW	2013/10/17	COMPAL	follow Dell requirement.	add back SUS_ON, change +3.3V_SUS control pin to SIO_SLP_S4# 1. UL3.3 from SIO_SLP_S4# to SUS_ON 2. UE2.B23 → SUS_ON_EC , RPE10.2 → SUS_ON 3. add RE282(Pop), RE281(depop) 4. add RE279, RE280 ( dock only) 5. UE2.B9 → RUN_ON_EC	0.2 (X01)
16	23	HW	2013/10/18	COMPAL	follow ESD recommend.	LZ1 change from SM070001N00 to SM070003Y00	0.2 (X01)
17	12	HW	2013/10/24	COMPAL	add GPIO pin for DIMM quantity detection.	add DIMM_DET on UC1.U4 to replace PCH_GPIO48, remove	0.2 (X01)
18	6	HW	2013/10/24	COMPAL	debug usage.	add RC301	0.2 (X01)
19	9	HW	2013/10/28	COMPAL	reserve it to prevent PCH_PLTRST# floating when power on	add RC304, 100K pull down, on PCH_PLTRST#_EC	0.2 (X01)
20	30	HW	2013/10/29	COMPAL	New SIM connector has no this pin.	remove UIM_DET on JNGFF2 pin58	0.2 (X01)
21	23	HW	2013/10/29	COMPAL	it's designed for Goliad, Houston doesn't need.	remove RZ1	0.2 (X01)
22	30	HW	2013/10/29	COMPAL	To solve WWAN can not detec issue.	Add RZ43, 100k pull up for WWAN_PWR_EN	0.2 (X01)
23	38	HW	2013/10/29	COMPAL	for support VPRO & NVPRO BOM option.	remove PJP33, PJP34, PJP19 add RZ44, RZ46, RZ47	0.2 (X01)
24	12	HW	2013/10/29	COMPAL	To solve backdrive issue.	Change TPM_PIRQ# pull up ( RC247) to +3.3V_RUN from +3.3V_ALW_PCH	0.2 (X01)
25	37	HW	2013/10/29	COMPAL	Dell request.	add RZ48, RZ49, QZ12 depop UZ5, UZ6, RZ21, RZ22, CZ35, RC91 (11/4) add RZ51, change QZ12 from 3904 to 3906. make RPE6 to be NC pin, add RE88 (11/4)	0.2 (X01)

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26	30	HW	2013/10/30	COMPAL	Dell doesn't support MODPHY.	add PJP36, depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.2 (X01)
27	28	HW	2013/11/04	COMPAL	SSI design will cause LED behavior error.	Change QL1, QL2 contorl pin from MASK_BASE_LEDS# to SYS_LED_MASK#	0.2 (X01)
28	21	HW	2013/11/04	COMPAL	EMC request.	Add RA42, RA43.	0.2 (X01)
29	21	HW	2013/11/05	COMPAL	follow vender suggestion. It's for 15KV ESD fail issue.	add CA12, CA13 change DA1, DA2, DA3, DA4 from GNDA to GND	0.2 (X01)
30	12	HW	2013/11/05	COMPAL	GPIO 14 is sus power well, it has risk to cause back drive.	move TPM_PIRQ# from PCH_GPIO14 to PCH_GPIO17, add T21 on PCH_GPIO14	0.2 (X01)
31	30	HW	2013/11/05	COMPAL	follow vender request.	RZ43 from 100K change to 0 ohm	0.2 (X01)
32	20	HW	2013/11/06	COMPAL	For SATA repeater setting	RN11,RN16 pop 0ohm	0.2 (X01)
33	28	HW	2013/11/06	COMPAL	For EMI request	RL21~ RL28 change to 2.2 ohm	0.2 (X01)
41	20	HW	2013/11/06	COMPAL	For SATA repeater setting	RN11,RN16 pop 0ohm	0.2 (X01)
42	30	HW	2013/11/05	COMPAL	follow vender request.	RZ43 from 100K change to 0 ohm	0.2 (X01)
43	9, 11, 27, 35, 36	HW	2013/11/20	COMPAL	follow vender suggest to solve "Bo" noise issue	1.UA1 pin22 add RA45 0 ohm PU to +3.3V_RUN_AUDIO 2.UA1 pin21 add RA44 100K ohm to GND	0.2 (X01)
44	12, 22	HW	2013/11/20	COMPAL	follow vender suggest	1.RPC8 change from 2.2k to 10K 2.UC1.F2 &RPC8.3 change name from I2C0_SDA to PCH_GPIO4 3.UC1.F3 &RPC8.4 change name from I2C0_SCL to PCH_GPIO5 4.UC1.G4 &RPC8.1 change name from I2C1_SDA_VMM to PCH_GPIO6 5.UC1.F1 &RPC8.2 change name from I2C1_SCL_VMM to PCH_GPIO7 6.RPV2.1 connect to I2C1_SDA_VMM 8.RPV2.2 connect to I2C1_SCL_VMM	0.2 (X01)
45	22	HW	2013/11/27	COMPAL	To solve CRT display jitter issue	LV23,LV25 change from BLM15AX102SN1D to BLM15PX181SN1D	0.2 (X01)
46	36, 37	HW	2013/11/27	COMPAL	Base on Pre-PT RSMRST EA result	1.POP RE88,UZ6,RE51 2.remove QZ12,RZ48,RZ49,RZ50	0.2 (X01)
47	6	HW	2013/11/29	COMPAL	follow intel DG, ESR MAX=50 ohm	Change YC1 from SJ100001K00(S CRYSTAL 32.768KHZ Q13FC1350000400) to SJ10000LD00(S CRYSTAL 32.768KHZ 12.5PF 9H03220008)	0.2 (X01)
48	22	HW	2013/12/10	COMPAL	follow vender suggestion	1. change LV22,LV24 from SM01000N400(S SUPPRE_MURATA BLM15AX102SN1D 0402) to SM01000N000(S SUPPRE_MURATA BLM15PX181SN1D 0402) 2. change CV82, CV94 from 1uF to 10uF 3. UV8 pin D3 from +1.05V_VMM_VDDTX to+1.05V_VMM_VDD. 4. UV8 Pin H3, E10, H11 change to NC 5. Change UV8 pin B5, B6 from +3.3V_RUN_VMM to +3.3V_RUN_VDDIO	0.2 (X01)

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49	34	HW	2013/12/18	COMPAL	To solve Power leakage issue.	Change R272 from 10K to 100K, and pull up to +3.3V_ALW2	0.2 (X01)
50	21	HW	2013/11/05	COMPAL	follow ESD/vender request	1. change RA42, RA43 to LA10, LA1 SM01000NA00(S SUPPRE_MURATA BLM15PX330SN1D 0402) 2. change RA7, RA8 from 16 to 24.9 ohm 3. DA1 &DA3 change from SCA00002900 to SCA00001B00(S ZEN ROW AZ5123-02S.R7G 3P C/A SOT23) 4.CA4&CA1 change from 220pF(@EMC@) to 680pF(EMC@)	0.2 (X01)
51	26	HW	2013/12/18	COMPAL	Base on CRT EA result	change CV51, CV52, CV53 from 12pF to 2.2pF	0.2 (X01)
52	20	HW	2013/12/18	COMPAL	For SATA repeater setting	De-pop RN9,RN13	0.2 (X01)
53	38	HW	2014/02/06	COMPAL	For MODPHY power rail contril by JUMP directly	1.change PJP36 pin1 from +1.05V_M to +1.05V_RUN 2.depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.3 (X01)
54	25	HW	2014/02/06	COMPAL	Base on PS8338 datasheet, PI0 have 2 level, PI1 have 3 level	For PI0, delete RV66 For PI1, add RV100 PD to GND	0.3 (X01)
55	36	HW	2014/02/10	COMPAL	EC request, for Delray common code reserved.	add RE283(@)	0.3 (X01)
56	29	HW	2014/02/27	COMPAL	EMI test fail , back to SSI SD card connector.	change JSD1 from TAITW_PSDCT6-20GLBS1NN4H 19P-T to ALPS_SCDADA0101_19P_NR	0.3 (X01)
57	9,16	HW	2014/03/03	COMPAL	follow intel DG 1.2	1.reserved 0.47uF for +PCH_VCCDSW3_3 , near CPU AH10 pin 2.add 10K pull high to +PCH_VCCDSW3_3 for PM_LANPHY_ENABLE, leave RPC19. pin 3 NC	0.3 (X01)
58	30	HW	2014/03/05	COMPAL	intel Wigig need 32K clock when DSx	1.Add UZ11&RZ56(@)&RZ57 2.JNGFF1 change to WIGIG_32KHZ from SUSCLK 3.JNGFF2.60 change to NC from SUSCLK	0.3 (X01)
59	27	HW	2014/03/05	COMPAL	EMC team Solution	1. reserved CZ68 47nF on pltrst_ush# to GND. 2. Pop R6,R41,R273 to 10 ohm 3. Pop C42,C43,C319 to 4.7pF	0.3 (X01)

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